
GC500-TS28IP

8-bit Turbo Microcontroller

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1 GC500-TS28IP Overview

1.1 General Description

GC500-TS28IP is a high-speed 80C52 compatible Microcontroller. It executes all of the conventional 80C52 instructions.

GC500-TS28IP has three timer/counters, maximum 24 programmable I/O pins, 10-channel 8-bit PWMs, Watchdog timer, POR (Power-On Reset), UART, 2-channel I2C, SPI, 16-channel 12-bit ADC and LVD (Low Voltage Detector) as peripherals. In addition, it contains an internal ring oscillator, which can generate the 48 MHz system clock signal instead of a crystal oscillator.

GC500-TS28IP operates over the extended -40°C to +125°C temperature range, and is available in the 28-pin TSSOP package.

1.2 Features

- ◆ CPU
 - 8-bit Turbo 80C52 Architecture
 - 4 Cycles / 1 Machine Cycle
 - Instruction Level Compatible with Intel 80C52
- ◆ Memory
 - 32KB Flash (Including 1KB User EEPROM)
 - 1KB Internal Aux. RAM
 - 256B Internal RAM
- ◆ Power Supply
 - Operating Voltage : +2.70V to +3.60V
- ◆ Operating Frequency : Max. 48MHz
- ◆ 24 Programmable I/O Pins
- ◆ 10-channel 8-bit PWMs

- ◆ Communication interfaces
 - 2-channel I2C Communication
 - 1-channel UART Communication
 - 1-channel SPI Communication
- ◆ 16-channel 12-bit ADC
- ◆ Internal Ring OSC with Calibration function
- ◆ Supporting ISP/IAP/MDS
- ◆ 9 Internal Interrupt Sources and 5 External Interrupt Sources
- ◆ 4 Reset Sources
- ◆ Power Down Wake-up Sources
 - Reset Sources + 5 External Interrupt (Both Levels)
 - Watchdog Timer Interrupt
- ◆ 3 operating modes : Active, Sleep, Deep Sleep
- ◆ E.S.D. Protection up to
 - 8,000V
- ◆ Latch-up Protection Up to $\pm 200\text{mA}$
- ◆ Package
 - 28-TSSOP

1.3 Applications

- ◆ Home appliance: TV, Monitor, Home Theater
- ◆ Mobile Phones
- ◆ Portable MP3, MP4
- ◆ Digital Cameras
- ◆ Battery power applications

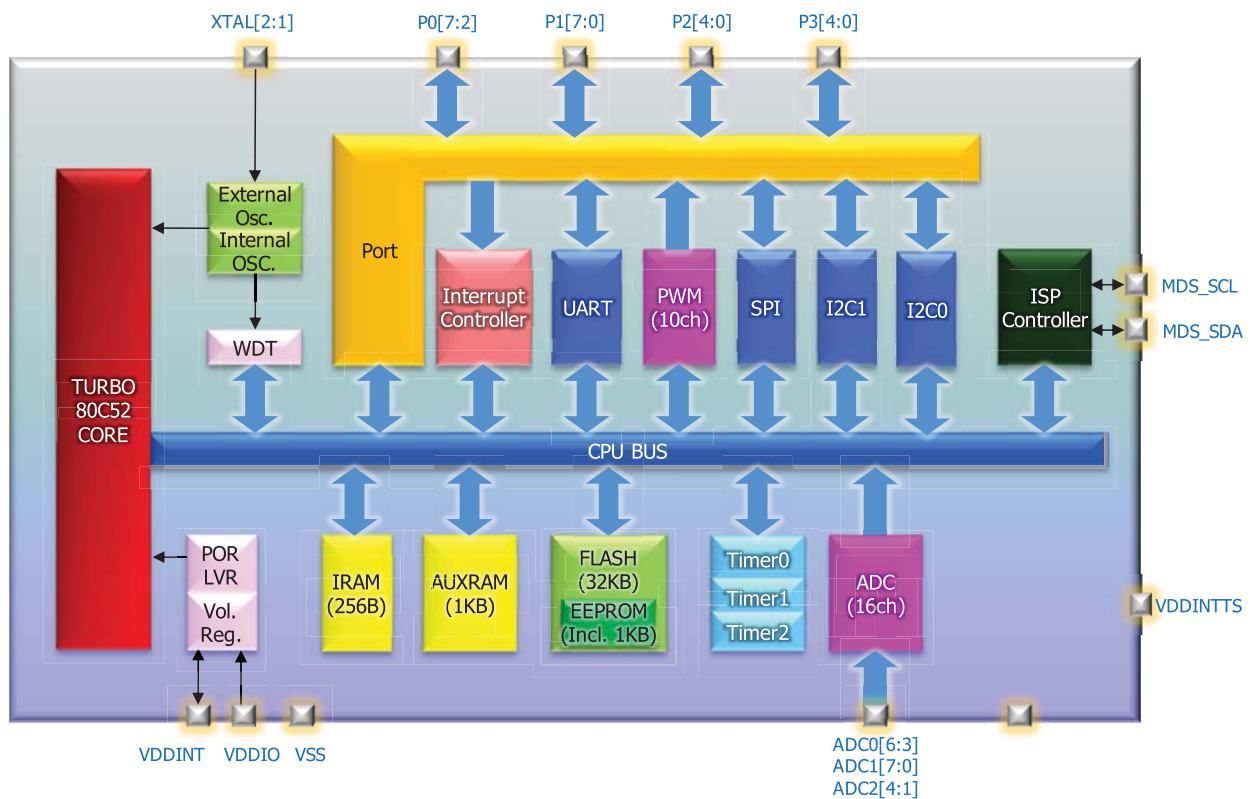
1.4 Product Family Guide

Product	Flash [Byte]	RAM [Byte]	ADC (bit X Ch)	PWM (bit X Ch)	I/O Pins	Package	Other Peripherals
GC500-TS28IP	32K	1K + 256	12 X 16	8 X 10	24	28-TSSOP	IAP ISP EJTAG 2 T/C [16bits] 1 SPI 2 I2C 1 UART WDT LVD POR RING
GC510-ML32IP	16K	1K + 256	12X 24	8 X 12	29	32- MLF(5x5,0.85T)	
GC520-ML32IP	8K	1K + 256	12 X 24	8 X 12	29	32- MLF(5x5,0.85T)	

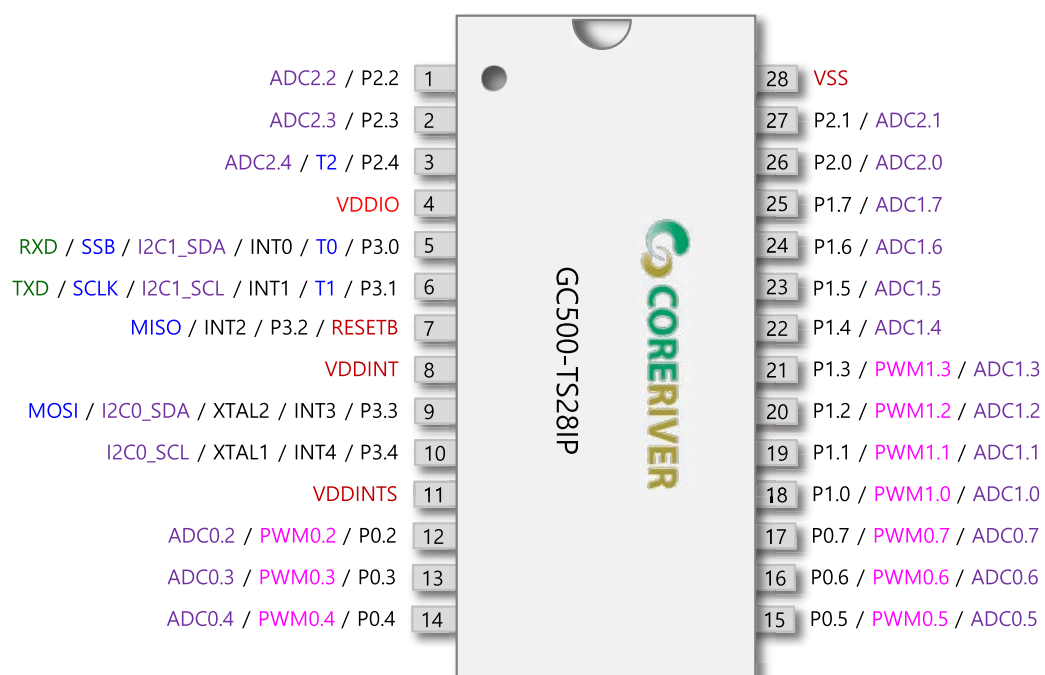
2 Block Diagram

Figure shows the block diagram of **GC500-TS28IP**. Programs reside in the internal program memory (Embedded Flash Memory). Data are read from or written to data memory (SRAM) or special function registers (SFRs).

The internal registers of **GC500-TS28IP** are configured as part of the on-chip RAM: therefore each register has an address. This is reasonable for **GC500-TS28IP**, since it has so many registers.



3 Pin Configuration



28-pin TSSOP Package Diagram

4 Pin Description

Pin No.	Name	Type	Description	Share Pins
1	P2.2	I/O	General I/O Port 2.2	ADC2.2
2	P2.3	I/O	General I/O Port 2.3	ADC2.3
3	P2.4	I/O	General I/O Port 2.4	ADC2.4 / T2
4	VDDIO	PWR		
5	P3.0	I/O	General I/O Port 3.0	RXD / SSB / I2C1_SDA / INT0 / T0
6	P3.1	I/O	General I/O Port 3.1	TXD / SCLK / I2C1_SCL / INT1 / T1
7	P3.2	I/O	General I/O Port 3.2	MISO / INT2 / RESETB
8	VDDINT	O	Digital Power Filter (+1.8V)	
9	P3.3	I/O	General I/O Port 3.3	MOSI / I2C0_SDA / XTAL2 / INT3
10	P3.4	I/O	General I/O Port 3.4	I2C0_SCL / XATL1 / INT4
11	VDDINTS	O	Digital Power Filter	
12	P0.2	I/O	General I/O Port 0.2	PWM0.2 / ADC0.2
13	P0.3	I/O	General I/O Port 0.3	PWM0.3 / ADC0.3
14	P0.4	I/O	General I/O Port 0.4	PWM0.4 / ADC0.4
15	P0.5	I/O	General I/O Port 0.5	PWM0.5 / ADC0.5
16	P0.6	I/O	General I/O Port 0.6	PWM0.6 / ADC0.6
17	P0.7	I/O	General I/O Port 0.7	PWM0.7 / ADC0.7
18	P1.0	I/O	General I/O Port 1.0	PWM1.0 / ADC1.0
19	P1.1	I/O	General I/O Port 1.1	PWM1.1 / ADC1.1
20	P1.2	I/O	General I/O Port 1.2	PWM1.2 / ADC1.2
21	P1.3	I/O	General I/O Port 1.3	PWM1.3 / ADC1.3
22	P1.4	I/O	General I/O Port 1.4	ADC1.4
23	P1.5	I/O	General I/O Port 1.5	ADC1.5
24	P1.6	I/O	General I/O Port 1.6	ADC1.6
25	P1.7	I/O	General I/O Port 1.7	ADC1.7
26	P2.0	I/O	General I/O Port 2.0	ADC2.0
27	P2.1	I/O	General I/O Port 2.1	ADC2.1
28	VSS	GND		

5 Absolute Maximum Ratings

.Absolute Maximum Ratings(TA = 25 °C)

Item	Conditions	Range
DC Voltage in V _{DDIO} relative to Ground	-	-0.5 V to +4.6V
DC Input Voltage	-	-0.5V to (V _{DDIO} +0.5V)
DC Output Voltage	-	-0.5 V to (V _{DDIO} +0.5V)
DC Output Current High	One I/O pin active	-25mA
	All I/O pin active	-100mA
DC Output Current Low	One I/O pin active	+30mA
	All I/O pin active	+150mA
Storage Temperature	-	-65 °C to +150 °C
Soldering Temperature	-	260 °C for 10 seconds

.Recommended Operating Conditions

Item	Conditions	Range
Operating Voltage	-	+2.7 V to +3.6V
Operating Temperature	-	-40 °C to + 125 °C

6 DC Characteristics

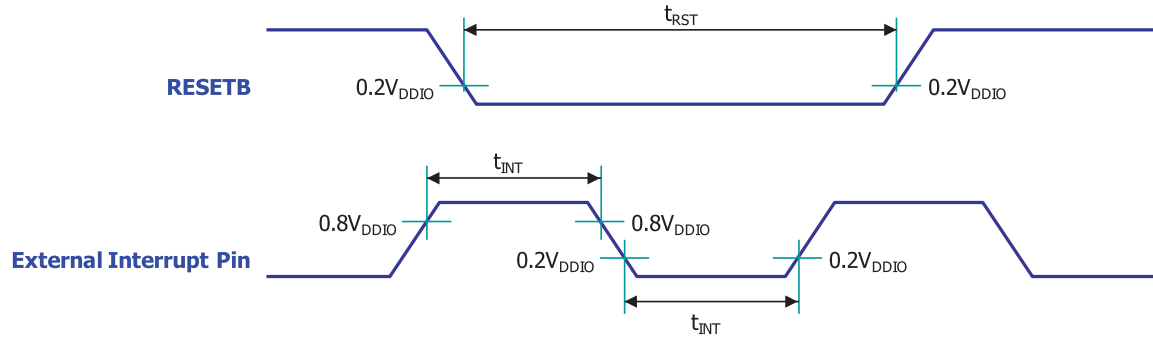
* $T_A = -40^{\circ}\text{C} \sim +125^{\circ}\text{C}$, $V_{DDIO} = 2.7\text{V} \sim 3.6\text{V}$ unless otherwise specified

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Input Low Voltage	V_{IL}	P0,P1,P2,P3	$V_{DDIO} = 2.7\text{V} \sim 3.6\text{V}$	-0.5	-	$0.2V_{DDIO} + 0.1$	V
Input high Voltage	V_{IH}	P0,P1,P2,P3	$V_{DDIO} = 2.7\text{V} \sim 3.6\text{V}$	$0.2V_{DDIO} + 1.0$	-	$V_{DDIO} + 0.5$	V
Output Low Voltage	V_{OL}	P0,P1,P2,P3	$V_{DDIO} = 3.0\text{V} \sim 3.6\text{V}$ ($I_{OL} = 4.35\text{mA}$) $V_{DDIO} = 2.7\text{V} \sim 3.0\text{V}$ ($I_{OL} = 3.55\text{mA}$)	-	-	$0.3V_{DDIO}$	V
		P0,P1,P2,P3[1:0] (High Drive)	$V_{DDIO} = 3.0\text{V} \sim 3.6\text{V}$ ($I_{OL} = 34.79\text{mA}$) $V_{DDIO} = 2.7\text{V} \sim 3.0\text{V}$ ($I_{OL} = 28.41\text{mA}$)	-	-	$0.3V_{DDIO}$	V
Output High Voltage	V_{OH}	P0,P1,P2,P3	$V_{DDIO} = 3.0\text{V} \sim 3.6\text{V}$ ($I_{OH} = -8.04\text{mA}$) $V_{DDIO} = 2.7\text{V} \sim 3.0\text{V}$ ($I_{OH} = -6.62\text{mA}$)	$0.7V_{DDIO}$	-	-	V
	V_{OHP}	P0,P1,P2,P3 (Pull-up Resistor Only)	$V_{DDIO} = 3.0\text{V} \sim 3.6\text{V}$ ($I_{OHP} = -30.30\mu\text{A}$) $V_{DDIO} = 2.7\text{V} \sim 3.0\text{V}$ ($I_{OHP} = -24.26\mu\text{A}$)	$0.7V_{DDIO}$	-	-	V
Logical 1 to 0 Transition Current	I_{TL}	P0,P1,P2,P3	$V_{DDIO} = 3.0\text{V} \pm 10\%$ ($V_{IN} = 2\text{V}$)	-	-	-650	μA
Input Leakage Current	I_{IL}	P0,P1,P2,P3	$V_{IN} = V_{IH}$ or V_{IL}	-	-	± 1	μA
Pin Capacitance	C_{IO}	All	$V_{DDIO} = 3.0\text{V}$	-	10	-	pF

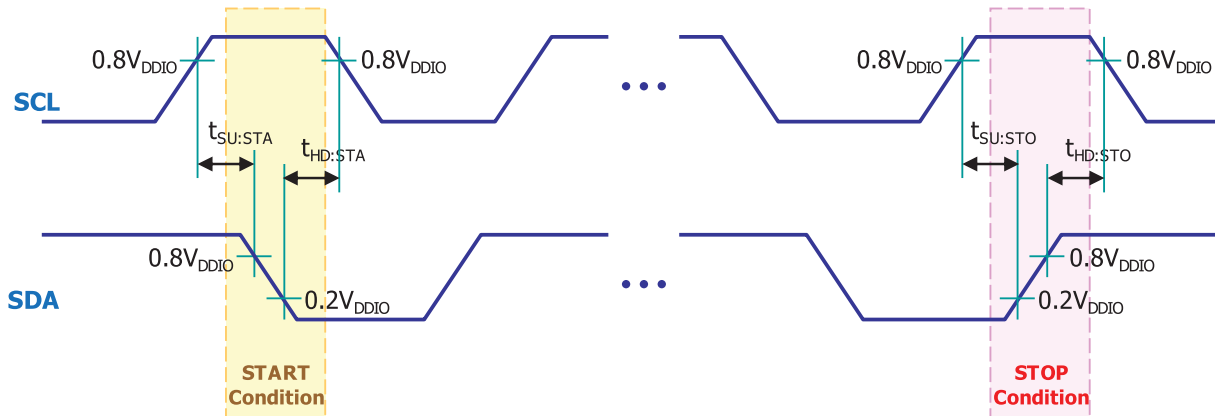
7 AC Characteristics

* $T_A = -40\text{ }^{\circ}\text{C} \sim +125\text{ }^{\circ}\text{C}$, $V_{DDIO} = 2.7\text{V} \sim 3.6\text{V}$ unless otherwise specified

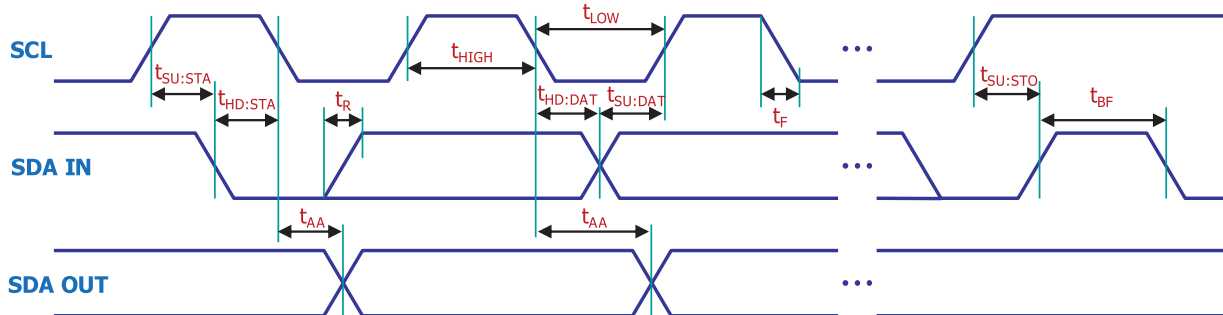
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
RESETB Input Width	t_{RST}	RESETB	$V_{DDIO} = 3\text{V} \pm 10\%$	24	-	-	F_{SYS}
External Interrupt Input Width	t_{INT}	External Interrupt	$V_{DDIO} = 3\text{V} \pm 10\%$	4	-	-	F_{SYS}



8 I2C Timing Characteristics



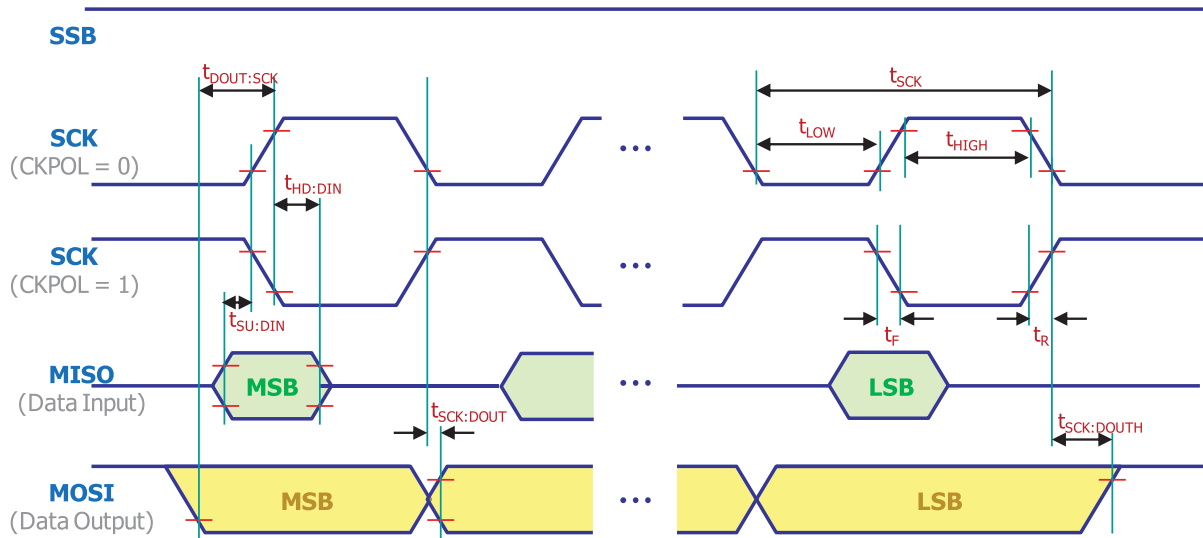
Symbol	Characteristics		Min. [ns]	Max. [ns]	Conditions
$t_{SU:STA}$	START Condition Setup Time	100kHz Mode	4,700	-	Only relevant for repeated START condition
		400kHz Mode	600	-	
$t_{HD:STA}$	START Condition Hold Time	100kHz Mode	4,700	-	After this period, the first clock pulse is generated
		400kHz Mode	600	-	
$t_{SU:STO}$	STOP Condition Setup Time	100kHz Mode	4,700	-	
		400kHz Mode	600	-	
$t_{HD:STO}$	STOP Condition Hold Time	100kHz Mode	4,700	-	
		400kHz Mode	600	-	



Symbol	Characteristics	Min. [ns]	Max. [ns]	Conditions	
t_{HIGH}	Clock High Time	100kHz Mode	4,000	-	Minimum Frequency : 1MHz
		400kHz Mode	600	-	Minimum Frequency : 5MHz
t_{LOW}	Clock Low Time	100kHz Mode	4,700	-	Minimum Frequency : 1MHz
		400kHz Mode	1,300	-	Minimum Frequency : 5MHz
$t_{SU:DAT}$	Data Input Setup Time	100kHz Mode	250	-	
		400kHz Mode	100	-	
$t_{HD:DAT}$	Data Input Hold Time	100kHz Mode	0	-	
		400kHz Mode	0	900	
t_{AA}	Data Valid from Clock	100kHz Mode	-	3,500	
		400kHz Mode	-	-	
t_{BF}	BUS Free Time	100kHz Mode	4,700	-	
		400kHz Mode	1,300	-	
t_R	SDA & SCL Rising Time	100kHz Mode	-	1,000	The Range of Cb is from 10pF to 400pF
		400kHz Mode	$2.0 + 0.1C_b$	300	
t_F	SDA & SCL Falling Time	100kHz Mode	-	300	The Range of Cb is from 10pF to 400pF
		400kHz Mode	$2.0 + 0.1C_b$	300	

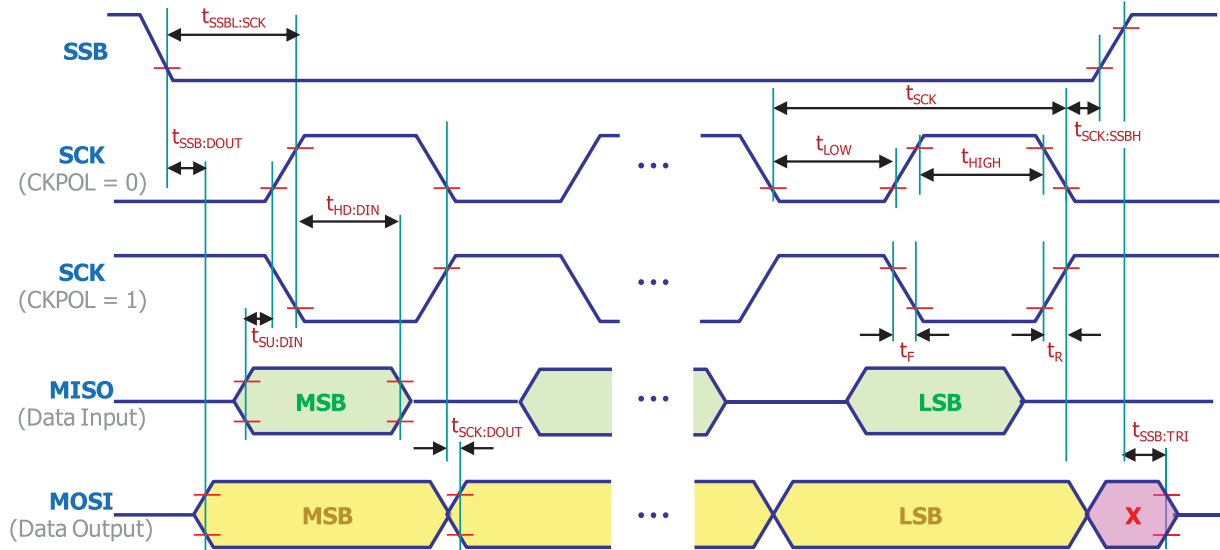
9 SPI Timing Characteristics

9.1 Master Mode



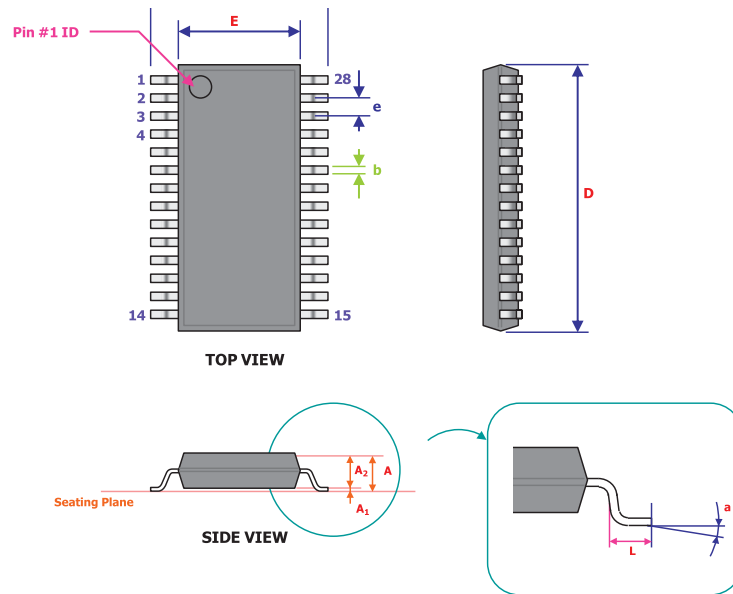
Symbol	Description	Mode	Min. [ns]	Typ. [ns]	Max. [ns]
t_{SCK}	SCK Period Time (using SFR 'SPICK')	Master	-	$F_{osc}/2 \sim F_{osc}/256$	-
t_{HIGH}, t_{LOW}	SCK High / Low	Master	-	50% Duty Cycle	-
t_F, t_R	SCK Rise / Fall Time	Master	-	3.6	-
$t_{SU:DIN}$	Data Input Setup Time	Master	-	10	-
$t_{HD:DIN}$	Data Input Hold Time	Master	-	10	-
$t_{DOUT:SCK}$	Data Output to SCK	Master	-	$0.5 \times t_{SCK}$	-
$t_{SCK:DOUT}$	SCK to Data Output	Master	-	10	-
$t_{SCK:DOUTH}$	SCK to Data Output High	Master	-	10	-

9.2 Slave Mode



Symbol	Description	Mode	Min. [ns]	Typ. [ns]	Max. [ns]
$t_{SSB:DOUT}$	SSB Low to Data Output	Slave	-	15	-
T_{SCK}	SCK Period Time	Slave	$4 \times t_{Sys}$	-	-
t_{HIGH}, t_{LOW}	SCK High / Low	Slave	$2 \times t_{Sys}$	-	-
t_F, t_R	SCK Rise / Fall Time	Slave	-	1,600	-
$t_{SU:DIN}$	Data Input Setup Time	Slave	10	-	-
$t_{HD:DIN}$	Data Input Hold Time	Slave	t_{Sys}	-	-
$t_{SCK:DOUT}$	SCK to Data Output	Slave	-	15	-
$t_{SCK:SSBH}$	SCK to SSB High	Slave	20	-	-
$t_{SSB:TRI}$	SSB High to Tri-state	Slave	-	10	-
$t_{SSBL:SCK}$	SSB Low to SCK	Slave	20	-	-

10 28-pin TSSOP Package Dimension



Symbol	Dimensions [mm]		
	Min.	Nom.	Max.
A	-	-	1.20
A ₁	0.05	-	0.15
A ₂	0.80	-	1.00
D	9.60	-	9.80
E	4.30	-	4.50
E ₁	6.25	-	6.55
B	0.19	-	0.30
E	0.65 BSC		
L	0.50	0.60	0.70
a	1°	-	7°

Notes:

- All Dimension are in mm. Angles in Degrees.
- Dimension b applies to Plated Terminal & is measured.
- BSC : Basic Dimension. Theoretically exact value shown without tolerances.
REF : Reference Dimension, Usually without tolerance, for information purpose only.

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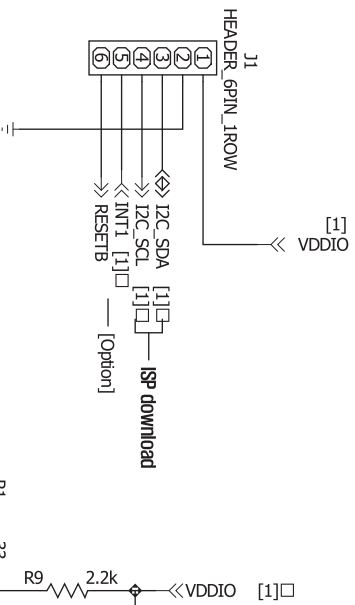
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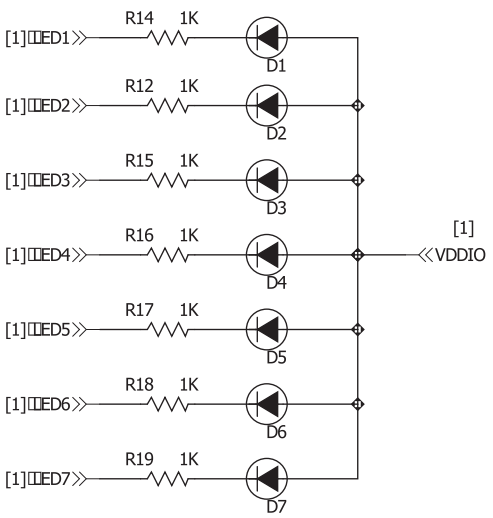
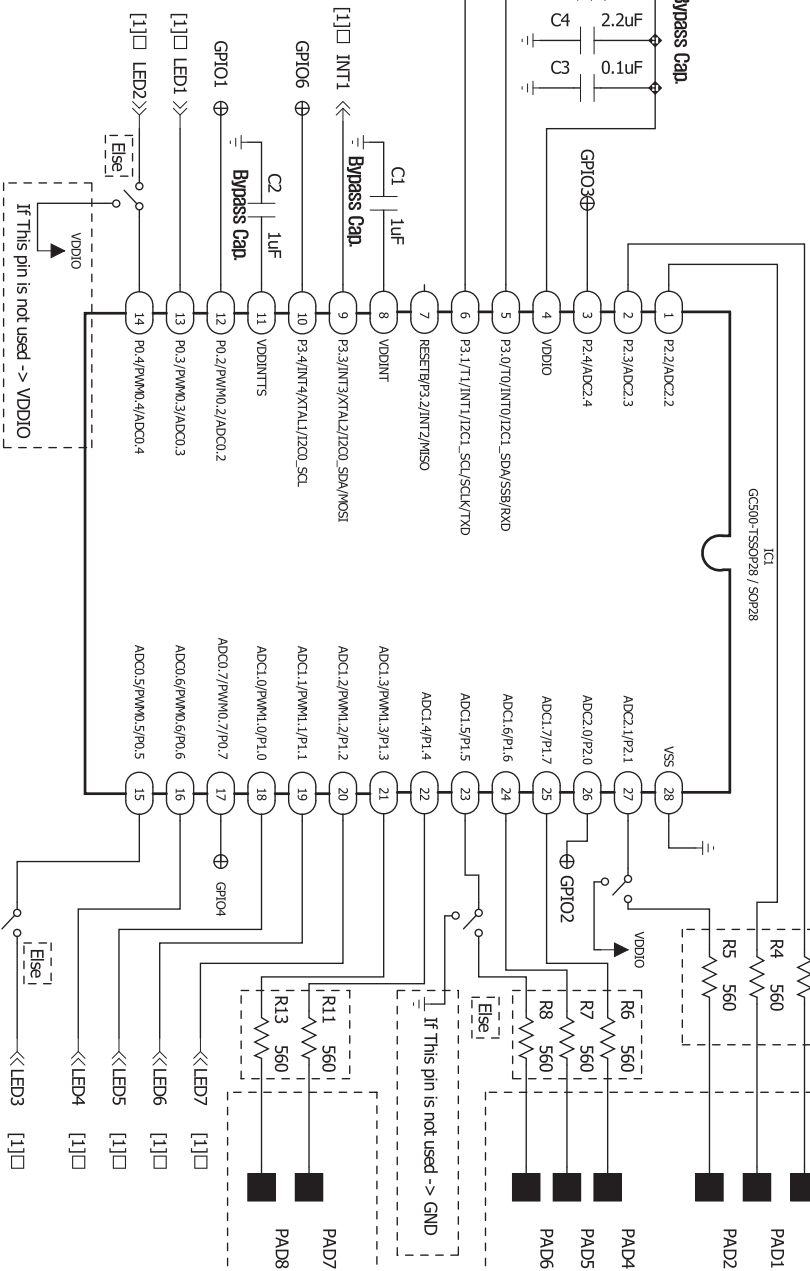
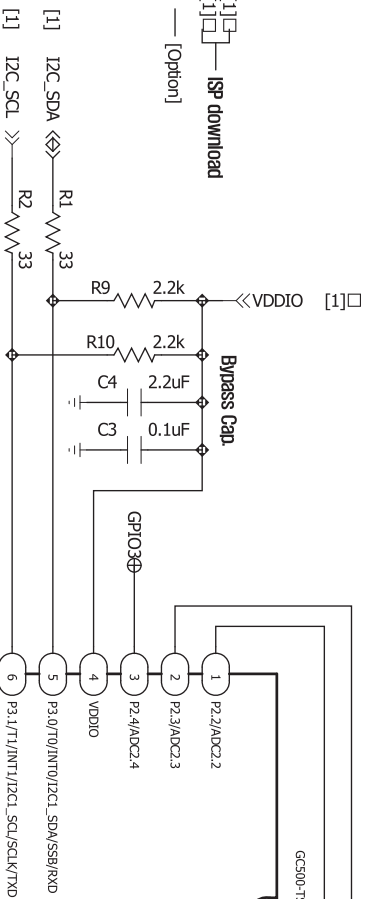
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GC500_TSSOP28 / SOP28

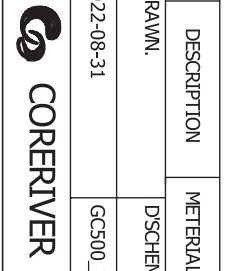
>> VDDIO (Operating Voltage) : +2.7V to +3.6V



ISP download External interface



NO.	REVISION NO.	NO.	REVISION NO.	C	B	A	NO	PART NO.	DESCRIPTION	MATERIAL	COLOR FINISH	NOTE
1							SCALE		DRAWN	DISCHHEMATIC		
2							A3		2022-08-31	GC500_TSSOP28_SOP28		
				QUANTITY			UNIT					
				SHEET			1	1				



A

B

C

D

E

A

B

C

D

E