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# GC221-TS20IP

## *8-bit Turbo Microcontroller*

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## 1 GC221-TS20IP Overview

### 1.1 General Description

**GC221-TS20IP** is a high-speed 80C52 compatible Microcontroller. It executes all of the conventional 80C52 instructions.

**GC221-TS20IP** has three timer/counters, 18 programmable I/O ports, Watchdog timer, Stop timer, POR (Power-On Reset), UARTs, I<sup>2</sup>Cs, and LVD (Low Voltage Detector) as peripherals. In addition, it contains an internal precision oscillator, which can generate the 12 MHz system clock signal instead of a crystal oscillator.

**GC221-TS20IP** operates over the extended -40°C to +85°C temperature range and is available in the 20-pin TSSOP package.

### 1.2 Features

- ◆ **CPU**
  - ✓ 8-bit turbo 80C52 architecture
  - ✓ 4 cycles/1 machine cycle
  - ✓ instruction level compatible with Intel 80C52
- ◆ **4 KB FLASH (Including 128B User EEPROM)**
- ◆ **Supporting ISP/IAP/MDS**
- ◆ **128B Internal RAM**
- ◆ **Operating Voltage : +2.2V to +5.5V**
- ◆ **Operating Frequency (F<sub>sys</sub>)**
  - ✓ 3.68 MHz (Internal POSC Clock, Default)
  - ✓ Max. 12 / 11.06 MHz @2.2V ~ 3.3V (External/Internal POSC Clock)
  - ✓ Max. 24 MHz @4.5V ~ 5.5V (External Clock)
- ◆ **Operating temperature : -40 °C ~ 85 °C**
- ◆ **18 Programmable I/O Pins**
  - ✓ Pull-up control, Open drain, & Push-Pull output
  - ✓ TTL and CMOS compatible logic levels

- ◆ **Configurable Low Voltage Detector (LVD)**
- ◆ **Internal Precision OSC with Calibration function**
  - ✓ 11.06 MHz @+2.2V to +5.5V (Typ. +/- 1%)
  - ✓ 32kHz @+2.7V (+/- 10%); Low Power OSC.
- ◆ **16-channel 10-bit ADC**
  - ✓ Max. 120k SPS @ $F_{ADC} = 12$  MHz ( $F_{SYS} = 12$  MHz)
  - ✓ Programmable Input Clock Frequency
- ◆ **23-bit Programmable Watchdog Timer**
- ◆ **16-bit Stop Timer**
- ◆ **Two 16-bit Timer/Counters**
- ◆ **Full-Duplex 1-channel UART Comm.**
- ◆ **1-channel I2C Comm. (I2C Slave)**
- ◆ **1-channel 10-bit high speed PWM**
- ◆ **12 Interrupt Sources**
  - ✓ Timer0/1, WDT, LVD, ADC, UART, PWM, I2C1
  - ✓ 4 External Interrupt Sources: Both Edge/Level
  - ✓ Two-level Interrupt Priority
- ◆ **Reset Sources**
  - ✓ On-chip Power-On-Reset (POR/LVR)
  - ✓ External Reset
  - ✓ Configurable Low Voltage Detector Reset
  - ✓ Watchdog Timer Reset
- ◆ **Power Down Wake-up Sources**
  - ✓ Reset Sources + 4 External Interrupt (Both Levels)
  - ✓ I2C Interrupt or WDT Interrupt
  - ✓ Stop Timer wake-up
- ◆ **Power Consumption**
  - ✓ Active Current: Max. 2mA @+3.0V, 2MHz
  - ✓ Stop Current1: Max. 1uA @+5.0V (All Clock OFF)
  - ✓ Stop Current2: Max. 450uA @+3.0V, 461kHz (Only WDT is on)
  - ✓ Stop Current3: Max. 5uA @+3.0V (Only ST is ON)
- ◆ **E.S.D. Protection up to 2,000 V**
- ◆ **Latch-up Protection Up to  $\pm 200$ mA**
- ◆ **Package**
  - ✓ 20-TSSOP

### 1.3 Applications

- ◆ Mobile Devices
- ◆ Multimedia
- ◆ Navigation Systems
- ◆ Home Appliance
- ◆ Other Electronic Devices

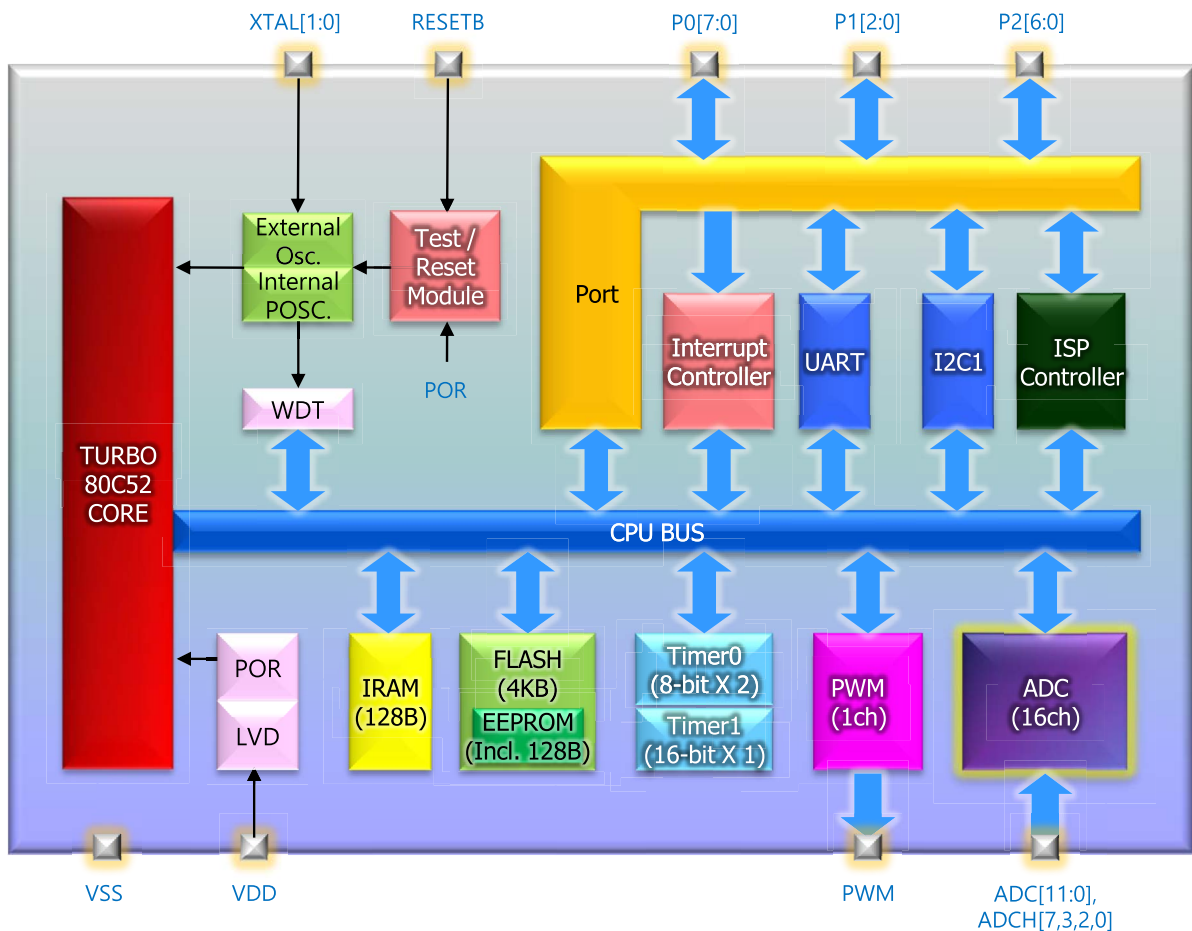
### 1.4 Product Family Guide

| Product      | Flash [Byte] | RAM [Byte] | Package                            | Programmable I/O     | Other Peripherals  |
|--------------|--------------|------------|------------------------------------|----------------------|--|
| GC220        | 8K           | 128        | 20-TSSOP                           | 18                   | 3 Timer/Counters<br>UART<br>I2C<br>WDT<br>IAP<br>ISP<br>EJTAG<br>LVD<br>POR<br>Precision Oscillator<br>Stop Timer<br>16-channel 10-bit ADC<br>1-channel 10-bit PWM |
| <b>GC221</b> | <b>4K</b>    | <b>128</b> | <b>20-TSSOP</b><br>16-SOP<br>8-SOP | <b>18</b><br>14<br>6 |  |
| GC222        | 2K           | 128        | 20-TSSOP                           | 18                   |  |

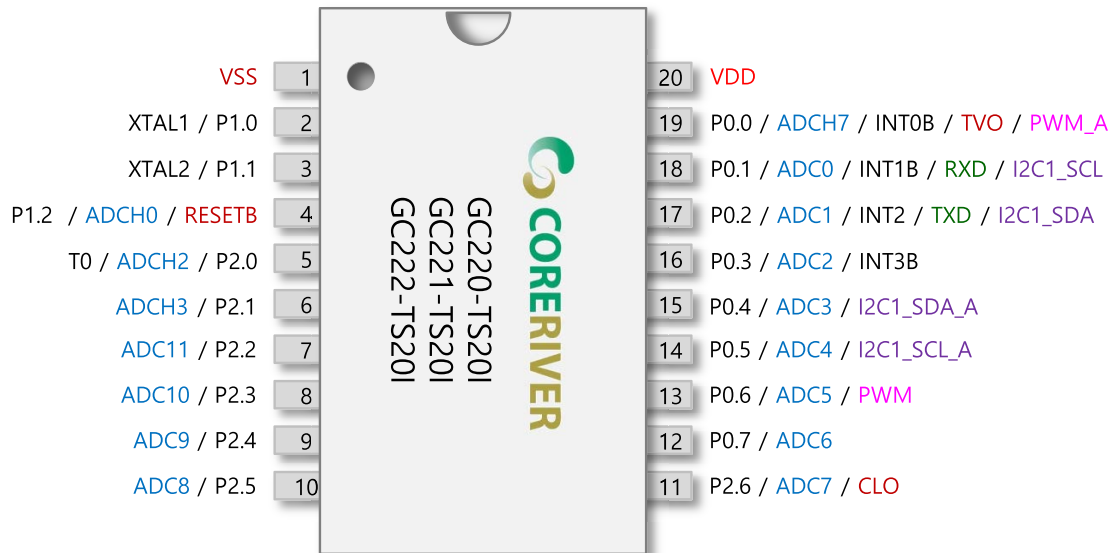
## 2 Block Diagram

Figure shows the block diagram of **GC221-TS20IP**. Programs reside in the internal program memory (Embedded Flash Memory). Data are read from or written to data memory (SRAM) or special function registers (SFRs).

The internal registers of **GC221-TS20IP** are configured as part of the on-chip RAM: therefore each register has an address. This is reasonable for **GC221-TS20IP**, since it has so many registers.



### 3 Pin Configuration



20-pin TSSOP Package Diagram

## 4 Pin Description

| Pin No. | Name   | Type | Description          | Share Pins                    |
|---------|--------|------|----------------------|-------------------------------|
| 1       | VSS    | GND  |                      |                               |
| 2       | XTAL1  | I/O  | Crystal Input        | P1.0                          |
| 3       | XTAL2  | I/O  | Crystal Output       | P1.1                          |
| 4       | RESETB | I/O  | External Reset Input | P1.2 / ADCH0                  |
| 5       | P2.0   | I/O  | General I/O          | T0 / ADCH2                    |
| 6       | P2.1   | I/O  | General I/O          | ADCH3                         |
| 7       | P2.2   | I/O  | General I/O          | ADC11                         |
| 8       | P2.3   | I/O  | General I/O          | ADC10                         |
| 9       | P2.4   | I/O  | General I/O          | ADC9                          |
| 10      | P2.5   | I/O  | General I/O          | ADC8                          |
| 11      | P2.6   | I/O  | General I/O          | ADC7                          |
| 12      | P0.7   | I/O  | General I/O          | ADC6                          |
| 13      | P0.6   | I/O  | General I/O          | ADC5 / PWM                    |
| 14      | P0.5   | I/O  | General I/O          | ADC4 / I2C1_SCL_A             |
| 15      | P0.4   | I/O  | General I/O          | ADC3 / I2C1_SDA_A             |
| 16      | P0.3   | I/O  | General I/O          | ADC2 / INT3B                  |
| 17      | P0.2   | I/O  | General I/O          | ADC1 / INT2 / TXD / I2C1_SDA  |
| 18      | P0.1   | I/O  | General I/O          | ADC0 / INT1B / RXD / I2C1_SCL |
| 19      | P0.0   | I/O  | General I/O          | ADCH7 / INT0B / TVO / PWM_A   |
| 20      | VDD    | PWR  |                      |                               |

## 5 Absolute Maximum Ratings

| Item                                   | Conditions         | Range   |
|--|--------------------|---|
| Voltage on any pin relative to Ground  | -                  | -0.5 V to ( $V_{DDIO}+0.5V$ )                           |
| Voltage in $V_{DD}$ relative to Ground | -                  | -0.5V to 6.5V   |
| Output Voltage                         | -                  | -0.5 V to ( $V_{DDIO}+0.5V$ )                           |
| Output Current High                    | One I/O pin active | -25mA   |
|  | All I/O pin active | -100mA  |
| Output Current Low                     | One I/O pin active | +30mA   |
|  | All I/O pin active | +150mA  |
| Storage Temperature                    | -                  | < 40°C  |
| Soldering Temperature                  | -                  | 260°C, 10 seconds within 5°C of actual peak temperature |



## 6 DC Characteristics

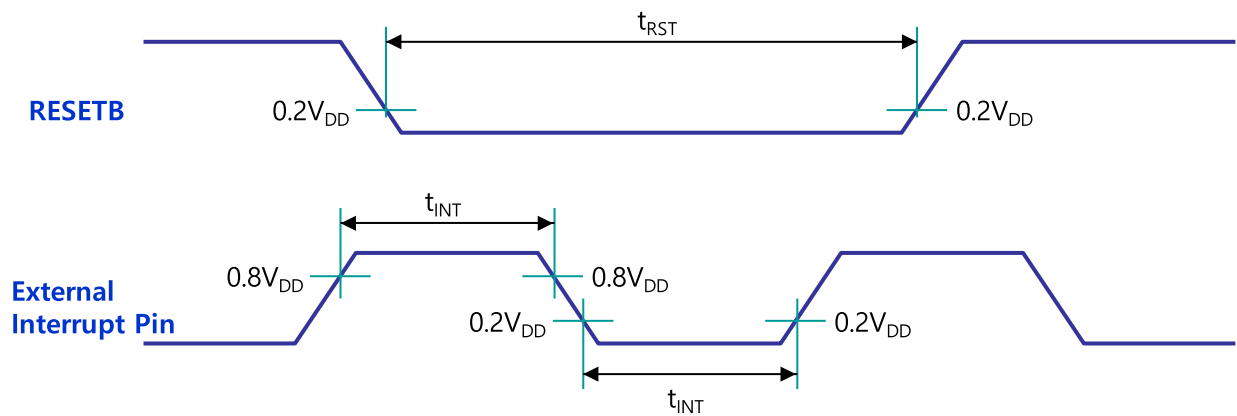
\*  $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$  unless otherwise specified

| Parameter             | Symbol    | Pin                                 | Conditions   | Value             |      |                   | Unit          |
|-----------------------|-----------|-------------------------------------|--|-------------------|------|-------------------|---------------|
|                       |           |                                     |  | Min.              | Typ. | Max.              |               |
| Input Low Voltage     | $V_{IL1}$ | RESETB ,P0, P1, P2                  | $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$  | -0.5              | -    | $0.2V_{DD} - 0.1$ | V             |
|                       | $V_{IL2}$ | XTAL1, XTAL2                        |  | 0.5               |      | $0.3V_{DD}$       |               |
| Input high Voltage    | $V_{IH1}$ | RESETB ,P0, P1, P2                  | $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$  | $0.2V_{DD} + 1.0$ | -    | $V_{DD} + 0.5$    | V             |
|                       | $V_{IH2}$ | XTAL1, XTAL2                        |  | $0.7V_{DD}$       | -    | $V_{DD} + 0.5$    |               |
| Output Low Voltage    | $V_{OL}$  | All Pins                            | $I_{OL} = 17\text{mA} @V_{DD}=5\text{V}$<br>$I_{OL} = 7\text{mA} @V_{DD}=3\text{V}$<br>$I_{OL} = 4\text{mA} @V_{DD}=2.4\text{V}$               | -                 | -    | $0.3V_{DDIO}$     | V             |
|                       | $V_{OL2}$ | P0[3:0] when high drive is enabled. | $I_{OL} = 50\text{mA} @V_{DD}=5\text{V}$<br>$I_{OL} = 20\text{mA} @V_{DD}=3\text{V}$<br>$I_{OL} = 12\text{mA} @V_{DD}=2.4\text{V}$             | -                 | -    | $0.3V_{DDIO}$     | V             |
| Output High Voltage   | $V_{OH}$  | All Pins                            | $I_{OH} = -18\text{mA} @V_{DD}=5\text{V}$<br>$I_{OH} = -6\text{mA} @V_{DD}=3\text{V}$<br>$I_{OH} = -3\text{mA} @V_{DD}=2.4\text{V}$            | $0.7V_{DDIO}$     | -    | -                 | V             |
|                       | $V_{OH2}$ | P0[3:0] when high drive is enabled. | $I_{OH} = -26\text{mA} @V_{DD}=5\text{V}$<br>$I_{OH} = -8\text{mA} @V_{DD}=3\text{V}$<br>$I_{OH} = -4\text{mA} @V_{DD}=2.4\text{V}$            | $0.7V_{DDIO}$     | -    | -                 | V             |
|                       | $V_{OHP}$ | ALL Pins (Pull-up Resistor Only)    | $I_{OHP} = -49\mu\text{A} @V_{DD}=5\text{V}$<br>$I_{OHP} = -28\mu\text{A} @V_{DD}=3\text{V}$<br>$I_{OHP} = -22\mu\text{A} @V_{DD}=2.4\text{V}$ | $0.7V_{DDIO}$     | -    | -                 | V             |
| Input Leakage Current | $I_{IL}$  | All Pins Except of XTAL1, XTAL2     | $V_{IN} = V_{IH}$ or $V_{IL}$  | -                 | -    | $\pm 1$           | $\mu\text{A}$ |
| Pin Capacitance       | $C_{IO}$  | All Pins                            | $V_{DD} = 5\text{V}$   | -                 | 10   | -                 | pF            |

## 7 AC Characteristics

\*  $T_A = -40\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$  unless otherwise specified

| Parameter                      | Symbol           | Pin                                 | Conditions                           | Value |      |      | Unit             |
|--------------------------------|------------------|-------------------------------------|--------------------------------------|-------|------|------|------------------|
|                                |                  |                                     |                                      | Min.  | Typ. | Max. |                  |
| Operating Frequency            | $F_{\text{SYS}}$ | Internal Oscillator<br>XTAL1, XTAL2 | $V_{\text{DD}} = 5\text{V} \pm 10\%$ | -     | -    | 24   | MHz              |
|                                |                  |                                     | $V_{\text{DD}} = 3\text{V} \pm 10\%$ | -     | -    | 12   |                  |
| RESETB Input Width             | $t_{\text{RST}}$ | RESETB                              | $V_{\text{DD}} = 5\text{V} \pm 10\%$ | 20    | -    | -    | $F_{\text{SYS}}$ |
|                                |                  |                                     | $V_{\text{DD}} = 3\text{V} \pm 10\%$ | 20    | -    | -    |                  |
| External Interrupt Input Width | $t_{\text{INT}}$ | External Interrupt                  | $V_{\text{DD}} = 5\text{V} \pm 10\%$ | 4     | -    | -    | $F_{\text{SYS}}$ |
|                                |                  |                                     | $V_{\text{DD}} = 3\text{V} \pm 10\%$ | 4     | -    | -    |                  |

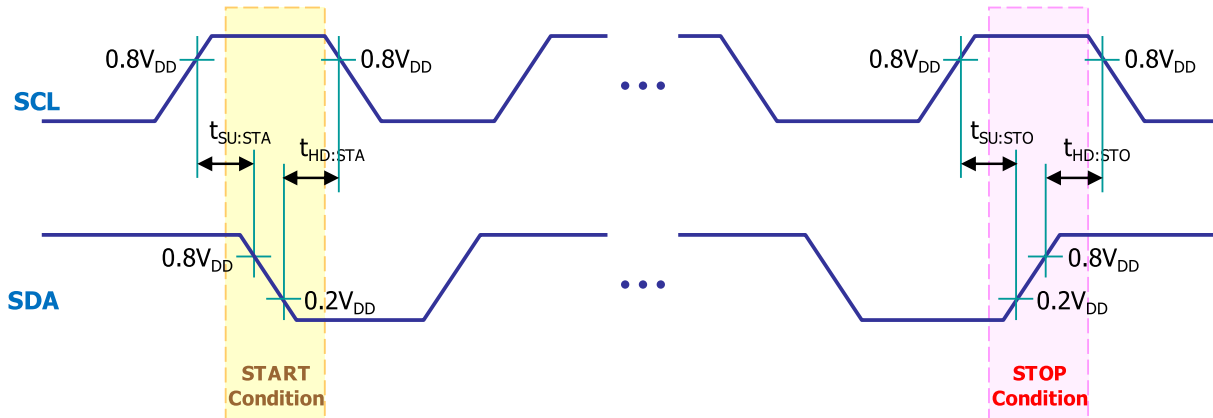


## 8 ADC Specifications

\*  $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$  unless otherwise specified

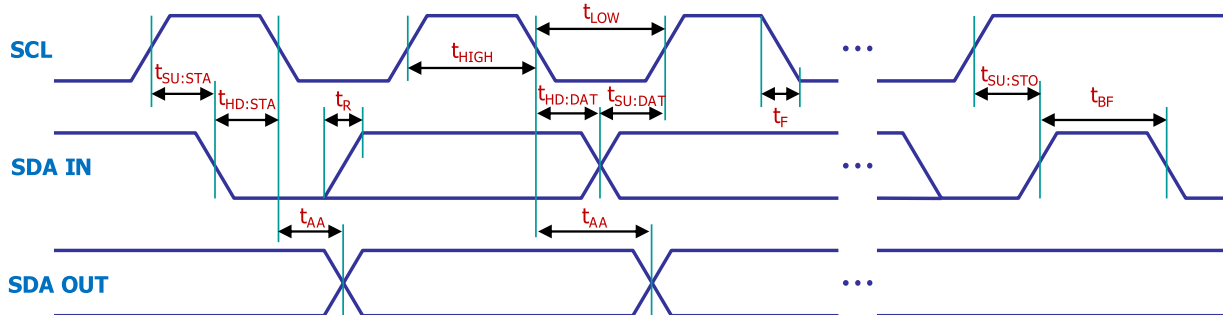
| Parameter                 | Symbol      | Conditions  | Value  |                |          | Unit |    |
|---------------------------|-------------|---|--|----------------|----------|------|----|
|                           |             |   | Min.   | Typ.           | Max.     |      |    |
| Supply Voltage            | $V_{DDADC}$ | $V_{DDADC} = V_{DD}$  | 2.4  | -              | 5.5      | V    |    |
| Input Voltage             | $V_{INADC}$ | -   | $V_{SS}$                                     | -              | $V_{DD}$ | V    |    |
| Resolution                | $RES_{ADC}$ | -   | -  | 10             | -        | bit  |    |
| Operating Frequency       | $F_{ADC}$   | $V_{DD} = 4.5\text{V} \sim 5.5\text{V}$<br>$V_{DD} = 2.4\text{V} \sim 3.3\text{V}$          | -  | -              | 10<br>5  | MHz  |    |
| Conversion Time           | $t_{ADC}$   | -   | -  | $96 / F_{ADC}$ | -        | s    |    |
| Overall Accuracy          | $OA_{ADC}$  | $V_{DD} = 5\text{V}, F_{ADC} = 10\text{MHz}$<br>$V_{DD} = 3\text{V}, F_{ADC} = 5\text{MHz}$ | -  | $\pm 2$        | $\pm 4$  | LSB  |    |
| Integral Nonlinearity     | $INL_{ADC}$ | $V_{DD} = 5\text{V}, F_{ADC} = 10\text{MHz}$<br>$V_{DD} = 3\text{V}, F_{ADC} = 5\text{MHz}$ | -  | $\pm 2$        | $\pm 4$  | LSB  |    |
| Differential Nonlinearity | $DNL_{ADC}$ | $V_{DD} = 5\text{V}, F_{ADC} = 10\text{MHz}$<br>$V_{DD} = 3\text{V}, F_{ADC} = 5\text{MHz}$ | -  | $\pm 0.5$      | $\pm 1$  | LSB  |    |
| Zero Input Error          | $ZIE_{ADC}$ | $V_{DD} = 5\text{V}, F_{ADC} = 10\text{MHz}$<br>$V_{DD} = 3\text{V}, F_{ADC} = 5\text{MHz}$ | -  | $\pm 2$        | $\pm 4$  | LSB  |    |
| Full Scale Error          | $FSE_{ADC}$ | $V_{DD} = 5\text{V}, F_{ADC} = 10\text{MHz}$<br>$V_{DD} = 3\text{V}, F_{ADC} = 5\text{MHz}$ | -  | $\pm 2$        | $\pm 4$  | LSB  |    |
| Analog Input Capacitance  | $C_{INADC}$ | -   | -  | 10             | 15       | pF   |    |
| ADC Current               | Active      | $I_{ADC}$   | $V_{DD} = 5\text{V}, F_{ADC} = 10\text{MHz}$ | -              | 1        | 2    | mA |
|                           |             |   | $V_{DD} = 3\text{V}, F_{ADC} = 5\text{MHz}$  | -              | 0.3      | 0.6  |    |
|                           | Power-down  | $V_{DD} = 5\text{V}$  | -  | -              | 100      | nA   |    |

## 9 I2C Timing Characteristics



\*  $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$  unless otherwise specified

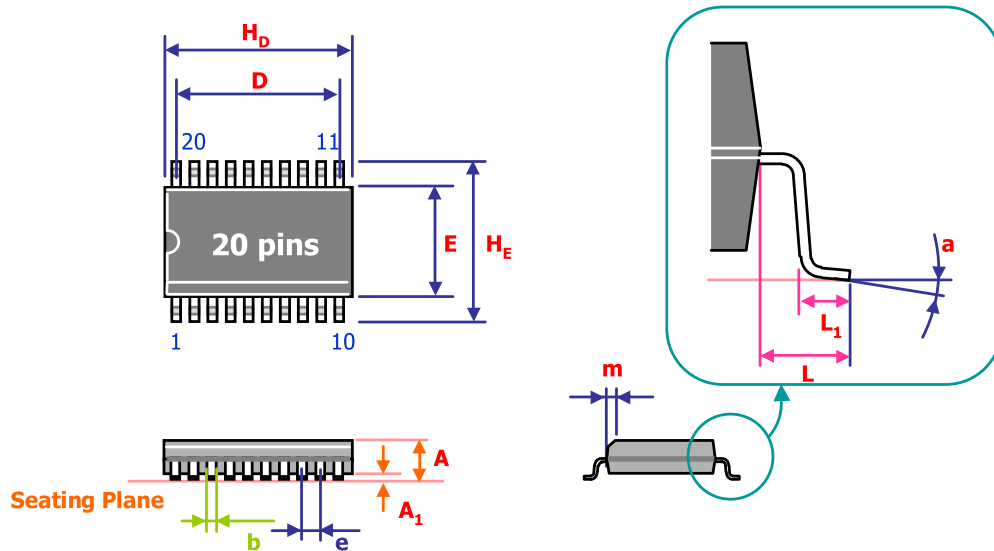
| Symbol       | Characteristics            |             | Min. [ns] | Max. [ns] | Conditions  |
|--------------|----------------------------|-------------|-----------|-----------|---|
| $t_{SU:STA}$ | START Condition Setup Time | 100kHz Mode | 4,700     | -         | Only relevant for repeated START condition            |
|              |                            | 400kHz Mode | 600       | -         |   |
| $t_{HD:STA}$ | START Condition Hold Time  | 100kHz Mode | 4,700     | -         | After this period, the first clock pulse is generated |
|              |                            | 400kHz Mode | 600       | -         |   |
| $t_{SU:STO}$ | STOP Condition Setup Time  | 100kHz Mode | 4,700     | -         |   |
|              |                            | 400kHz Mode | 600       | -         |   |
| $t_{HD:STO}$ | STOP Condition Hold Time   | 100kHz Mode | 4,700     | -         |   |
|              |                            | 400kHz Mode | 600       | -         |   |



\*  $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$  unless otherwise specified

| Symbol              | Characteristics        | Min. [ns]   | Max. [ns]      | Conditions |  |
|---------------------|------------------------|-------------|----------------|------------|--|
| $t_{\text{HIGH}}$   | Clock High Time        | 100kHz Mode | 4,000          | -          | Minimum Frequency : 1MHz                 |
|                     |                        | 400kHz Mode | 600            | -          | Minimum Frequency : 5MHz                 |
| $t_{\text{LOW}}$    | Clock Low Time         | 100kHz Mode | 4,700          | -          | Minimum Frequency : 1MHz                 |
|                     |                        | 400kHz Mode | 1,300          | -          | Minimum Frequency : 5MHz                 |
| $t_{\text{SU:DAT}}$ | Data Input Setup Time  | 100kHz Mode | 250            | -          |  |
|                     |                        | 400kHz Mode | 100            | -          |  |
| $t_{\text{HD:DAT}}$ | Data Input Hold Time   | 100kHz Mode | 0              | -          |  |
|                     |                        | 400kHz Mode | 0              | 900        |  |
| $t_{\text{AA}}$     | Data Valid from Clock  | 100kHz Mode | -              | 3,500      |  |
|                     |                        | 400kHz Mode | -              | -          |  |
| $t_{\text{BF}}$     | BUS Free Time          | 100kHz Mode | 4,700          | -          |  |
|                     |                        | 400kHz Mode | 1,300          | -          |  |
| $t_{\text{R}}$      | SDA & SCL Rising Time  | 100kHz Mode | -              | 1,000      | The Range of $C_b$ is from 10pF to 400pF |
|                     |                        | 400kHz Mode | $2.0 + 0.1C_b$ | 300        |  |
| $t_{\text{F}}$      | SDA & SCL Falling Time | 100kHz Mode | -              | 300        | The Range of $C_b$ is from 10pF to 400pF |
|                     |                        | 400kHz Mode | $2.0 + 0.1C_b$ | 300        |  |

## 10 20-pin TSSOP Package Dimension



| Symbol | Dimension in Inches |       |       | Dimension in mm |       |       |
|--------|---------------------|-------|-------|-----------------|-------|-------|
|        | Min.                | Nom.  | Max.  | Min.            | Nom.  | Max.  |
| A      |                     |       | 0.043 |                 |       | 1.1   |
| $A_1$  | 0.001               |       | 0.006 | 0.020           |       | 0.150 |
| b      | 0.007               |       | 0.012 | 0.190           |       | 0.300 |
| D      |                     | 0.234 |       |                 | 5.850 |       |
| E      | 0.169               | 0.174 | 0.177 | 4.300           | 4.400 | 4.500 |
| $H_D$  | 0.252               | 0.254 | 0.259 | 6.400           | 6.500 | 6.600 |
| $H_E$  | 0.246               | 0.252 | 0.258 | 6.250           | 6.400 | 6.550 |
| L      | 0.038               | 0.039 | 0.040 | 0.975           | 1.000 | 1.025 |
| $L_1$  | 0.020               | 0.024 | 0.028 | 0.500           | 0.600 | 0.700 |
| a      | 1°                  | -     | 7°    | 1°              | -     | 7°    |
| e      | 0.026 BSC           |       |       | 0.65 BSC        |       |       |

### Notes:

1. Dimension D & E include mold mismatch and are determined at the mold parting line.
2. General appearance spec. should be based on final visual inspection spec.