CORERIVER

Total Solution of MCU

MiDAS8000

Cortex-M0 Controller with LCD Driver

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1 MIDAS8000 Overview

1.1 General Description

MIDAS8000 is a high-performance 32-bit ARM Cortex-M0 compatible Processor.

MIDAS8000 has six timer/counters, maximum 87 programmable I/O pins, two 8-channel 10-bit PWMs, 2-channel 8bit PWM, 1 Watchdog timer, POR (Power-On Reset), five UARTs, I2C0, I2C1, SPI, maximum 16-channel ADC (Analog to Digital Converter), Comparator, Universal Remote Controller and LVD (Low Voltage Detector) as peripherals. In addition, it contains an internal precision oscillator and crystal pad.

MIDAS8000 operates over the extended -40℃ to +85℃ temperature range, and is available in the 68-pin QFN, 100-pin QFN package. On-chip SWD(Serial Wire Debugger) engine help to develop a system. Easy-to-use training kits are also provided.

1.2 Features

- Core
  - Cortex®-M0 CPU running at up to 66 MHz
  - ARMv6-M Architecture
  - Single-cycle hardware multiplier
- Memories
  - 256 KB in-system self-programmable Flash
  - 32 KB SRAM Memory
- Operating Voltage
  - Main power (VDDIO) : +2.35V to +5.5V
  - Analog power (VDDA) : +2.35V to +5.5V
  - Comm. power (VDDHOST) : +1.80V to +5.5V
- Operating Frequency
  - 66MHz / 44MHz / 22MHz (Dependent on the FCTRL.WAIT)
- Internal OSC with Calibration function
  - Precision Oscillator : 44MHz (±1%)
  - Low Power Oscillator : 10KHz (±10%)
- Supporting SWD (Serial Wire Debugger)

  - Processor halt, Single-step, Processor core register access
  - Reset and Hard Fault Vector Catch, full system memory access
  - 4 Breakpoint, 2 Watchpoint
- Three 16/8-bit Timer/Counters
- Two 32bit Timer/Counters & Dual Timer/Counter
- Two 8-channel 10-bit High Speed PWMs for LED Dimming
- 2-channel 10-bit High Speed PWMs for LED Dimming
- 32-bit Programmable Watchdog Timer
- 1-channel 12C0 Communication (Master/Slave)
- 1-channel I2C1 Communication (Slave Only)
- 24-bit Sleep Timer
- 1-channel SPI Communication (Master/Slave)
- 5-channel UART Communication
- 16-channel, 12-bit ADC
- Comparator
- Universal Remote Controller
- 4 COM x 44 SEG (or 4 COM x 32 SEG) LCD controller
- Exception Source
  - Watch dog timer (WDT)
  - Hard Fault
  - Supervisor Call (SVCall)
  - Pend able Service (Pend SV)
  - System Tick Timer (SYSTick)
- 31 IRQ Sources
  - Timer0/1/2/3/4, Dual Timer, PWM0/1/2
  - SPI, I2C0/1, UART0/1/2/3/4
  - COMP, LVD, UR, sleep timer, ADC, DMA, FLASH controller
  - 6 External Combination Interrupt
- Reset Sources
  - On-chip Power-On-Reset (POR)
  - External Reset
  - Low Voltage Detector Reset (LVR)
  - Watchdog Timer Reset
- Power Down Wake-up Sources

- Reset Sources + 6 GPIO Interrupt (Both Levels)
- Sleep Timer Interrupt

◆ Power Consumption

- Active Current : Down to 4mA @5.0V, POSC=24MHz
- IDLE Current : Down to 500uA @5.0V, POSC=24MHz
- SLEEP Current : Down to 5uA @2.35V, OSC32K=10KHz

◆ E.S.D. Protection up to 4,000V for All pin

◆ Latch-up Protection Up to ±200mA

◆ Package

- 100-QFN (12mm X 12mm)
- 68-QFN (8mm X 8mm)

1.3 Applications

◆ TV, Monitor, Home Theater

◆ Refrigerator, Washer, Air conditioner

◆ Battery power applications

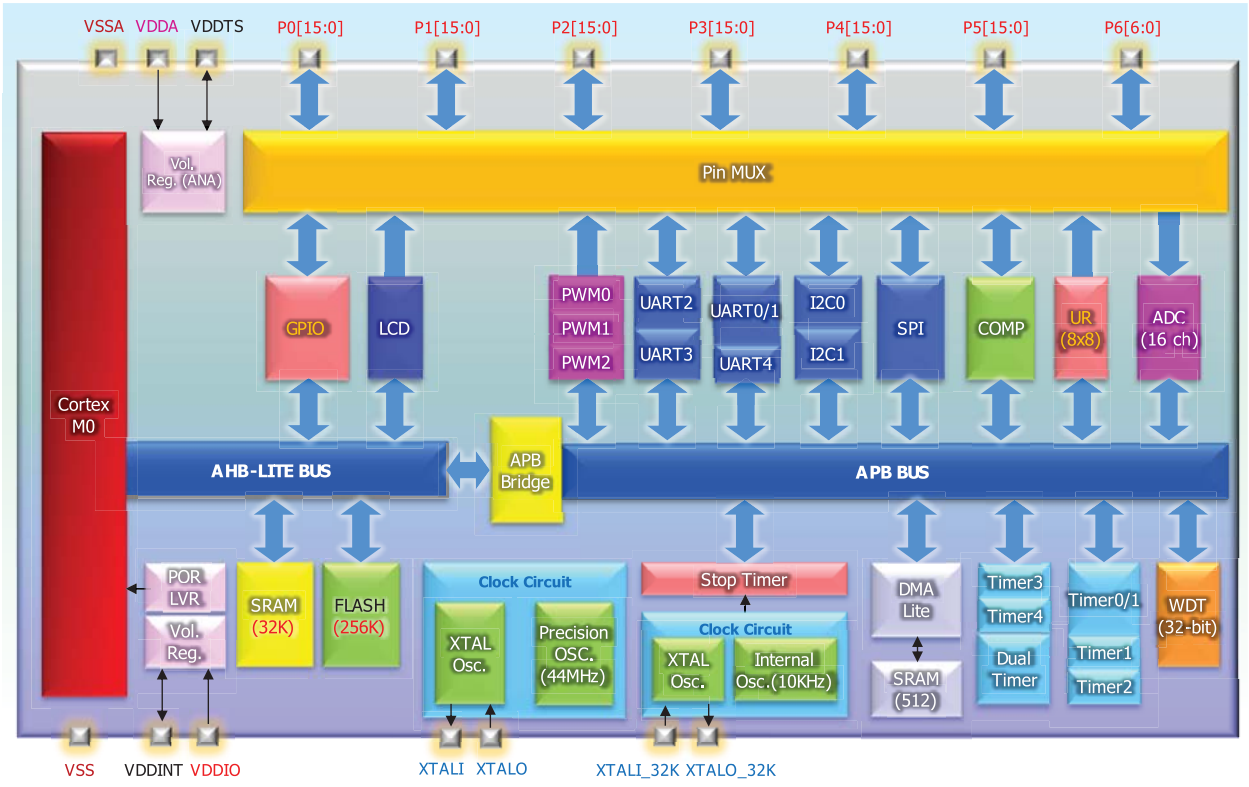
1.4 Product Family Guide

Product	Flash [Byte]	RAM [Byte]	LCD	ADC (bit x Ch)	PWM (bit x Ch)	I/O Pins	Package	Other Peripherals
GC8000-QF100IP	256K	32K	4 x 44	12 x 16	10 x 8 10 x 8 10 x 2	87	100-QFN (12x12, 0.85T)	IAP SWD 6 T/C 2 I2C 1 SPI 5 UART LCD ADC PWM WDT COMPARATOR LVD POR POSC XTAL
GC8000-QF68IP			4 x 32	12 x 9	10 x 6 10 x 8	56	68-QFN (8x8, 0.85T)	

2 Block Diagram

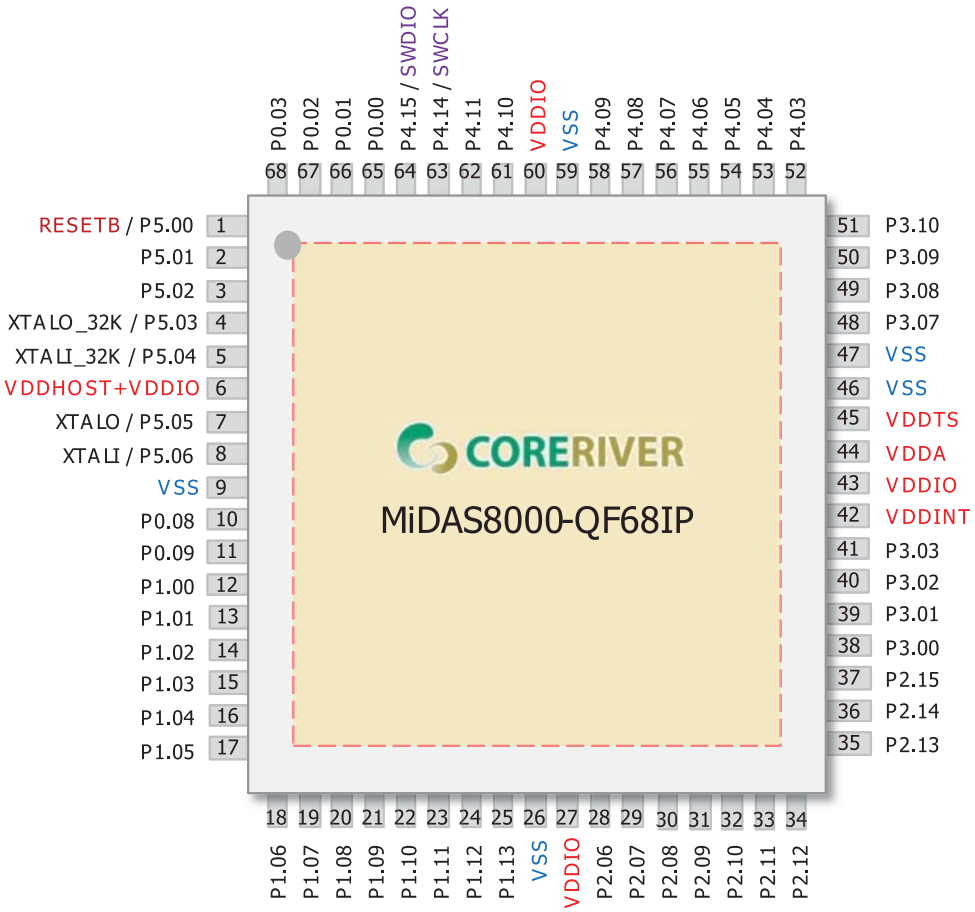
Figure shows the block diagram of ***MIDAS8000***. Programs reside in the internal program memory (Embedded Flash Memory). Data are read from or written to data memory (SRAM) or special function registers (SFRs).

The internal registers of ***MIDAS8000*** are configured as part of the on-chip RAM: therefore each register has an address. This is reasonable for ***MIDAS8000***, since it has so many registers.



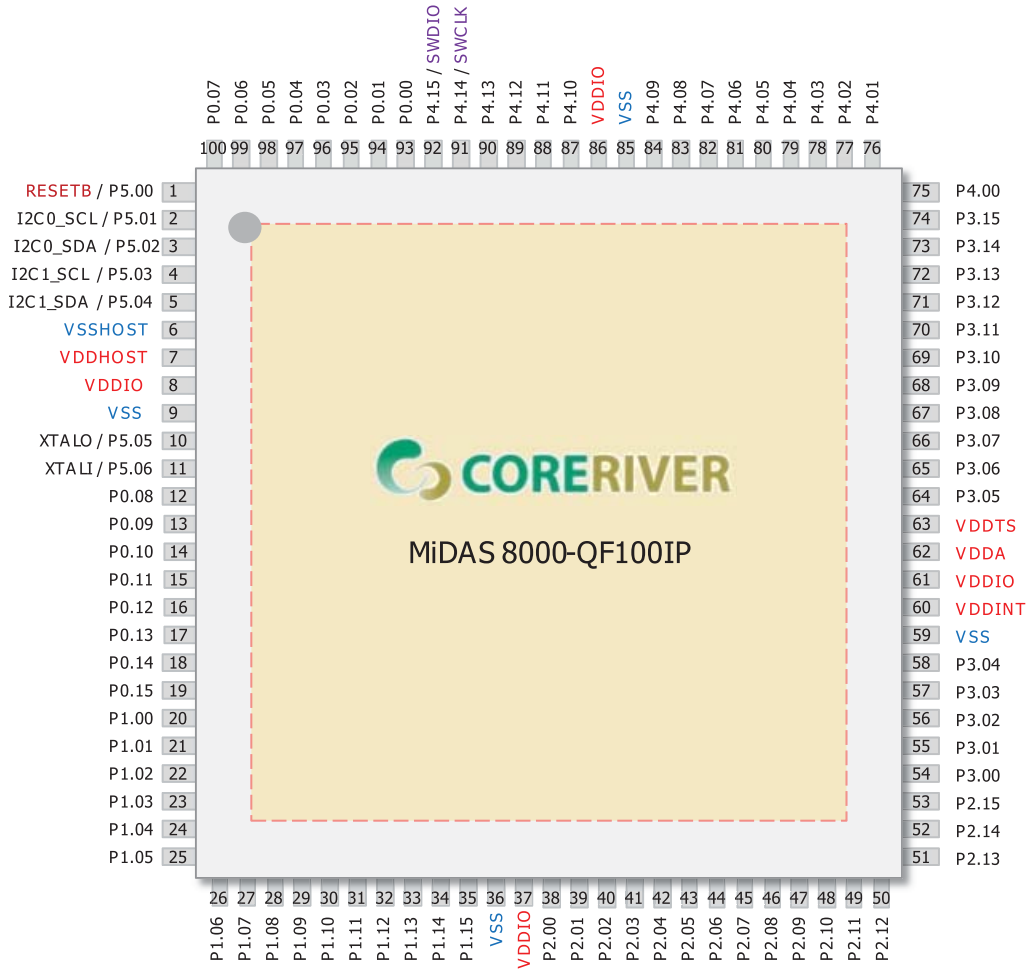
3 Pin Configuration

3.1 QFN 68 Pin



MIDAS8000-QF68IP Package Diagram

3.2 QFN 100 Pin



MIDAS8000-QF100IP Package Diagram

4 Pin Description

Symbol	Type	Description	Share Pins
VDDIO	PWR	Power Supply	-
VDDHOST	PWR	Power Supply for host interface (Port 5 IO Power)	-
VDDA	PWR	Analog IP Power Supply	-
VDDINT	O	Digital Power Filter (+1.5V)	-
VDDTS	O	Analog Power Filter	-
VSS	GND	Ground	-
VSSA	GND	Analog Ground	-
P5.00	I/O	General I/O Port 5.00	**RESETB**
P5.01	I/O	General I/O Port 5.01	I2C0_SCL / UART0_TxD
P5.02	I/O	General I/O Port 5.02	I2C0_SDA / UART0_RxD
P5.03	I/O	General I/O Port 5.03	XTALO_32 / I2C1_SCL / UART1_TxD
P5.04	I/O	General I/O Port 5.04	XTALI_32 / I2C1_SDA / UART1_RxD
P5.05	I/O	General I/O Port 5.05	XTALO / CLO
P5.06	I/O	General I/O Port 5.06	XTALI
P4.00	I/O	General I/O Port 4.00	ADC4 / PCOM0.0_A
P4.01	I/O	General I/O Port 4.01	ADC5 / PCOM0.1_A
P4.02	I/O	General I/O Port 4.02	ADC6 / PCOM0.2_A
P4.03	I/O	General I/O Port 4.03	ADC7 / PCOM0.3_A
P4.04	I/O	General I/O Port 4.04	ADC8 / PCOM0.4_A
P4.05	I/O	General I/O Port 4.05	ADC9 / PCOM0.5_A
P4.06	I/O	General I/O Port 4.06	ADC10 / PCOM0.6_A
P4.07	I/O	General I/O Port 4.07	ADC11 / PCOM0.7_A
P4.08	I/O	General I/O Port 4.08	ADC12 / PCOM1.0_A / COM0 / UART4_TxD
P4.09	I/O	General I/O Port 4.09	ADC13 / PCOM1.1_A / COM1 / UART4_RxD
P4.10	I/O	General I/O Port 4.10	ADC14 / PCOM1.2_A / COM2
P4.11	I/O	General I/O Port 4.11	ADC15 / PCOM1.3_A / COM3
P4.12	I/O	General I/O Port 4.12	PCOM1.4A / VLCD1
P4.13	I/O	General I/O Port 4.13	PCOM1.5A / VLCD2

P4.14	I/O	General I/O Port 4.14	PCOM1.6A / VLCD3 / SWCLK
P4.15	I/O	General I/O Port 4.15	PCOM1.7A / LVDD / SWDIO
P3.00	I/O	General I/O Port 3.00	SEG32 / I2C0_SCL_A
P3.01	I/O	General I/O Port 3.01	SEG33 / I2C0_SDA_A
P3.02	I/O	General I/O Port 3.02	SEG34 / COM_VN / I2C1_SCL_A
P3.03	I/O	General I/O Port 3.03	SEG35 / COM_VP / I2C1_SDA_A
P3.04	I/O	General I/O Port 3.04	SEG36 / REM
P3.05	I/O	General I/O Port 3.05	SEG37 / PWM2.0
P3.06	I/O	General I/O Port 3.06	SEG38 / PWM2.1
P3.07	I/O	General I/O Port 3.07	SEG39
P3.08	I/O	General I/O Port 3.08	SEG40
P3.09	I/O	General I/O Port 3.09	SEG41 / SWCLK_A
P3.10	I/O	General I/O Port 3.10	SEG42 / SWDIO_A
P3.11	I/O	General I/O Port 3.11	SEG43
P3.12	I/O	General I/O Port 3.12	ADC0
P3.13	I/O	General I/O Port 3.13	ADC1
P3.14	I/O	General I/O Port 3.14	ADC2
P3.15	I/O	General I/O Port 3.15	ADC3
P2.00	I/O	General I/O Port 2.00	SEG16 / PWM0.0_A
P2.01	I/O	General I/O Port 2.01	SEG17 / PWM0.1_A
P2.02	I/O	General I/O Port 2.02	SEG18 / PWM0.2_A
P2.03	I/O	General I/O Port 2.03	SEG19 / PWM0.3_A
P2.04	I/O	General I/O Port 2.04	SEG20 / PWM0.4_A
P2.05	I/O	General I/O Port 2.05	SEG21 / PWM0.5_A
P2.06	I/O	General I/O Port 2.06	SEG22 / PWM0.6_A
P2.07	I/O	General I/O Port 2.07	SEG23 / PWM0.7_A
P2.08	I/O	General I/O Port 2.08	SEG24 / PWM1.0_A
P2.09	I/O	General I/O Port 2.09	SEG25 / PWM1.1_A
P2.10	I/O	General I/O Port 2.10	SEG26 / PWM1.2_A / UART3_RxD
P2.11	I/O	General I/O Port 2.11	SEG27 / PWM1.3_A / UART3_TxD
P2.12	I/O	General I/O Port 2.12	SEG28 / PWM1.4_A / SPI_SSB_A
P2.13	I/O	General I/O Port 2.13	SEG29 / PWM1.5_A / SPI_SCK_A
P2.14	I/O	General I/O Port 2.14	SEG30 / PWM1.6_A / SPI_MISO_A

P2.15	I/O	General I/O Port 2.15	SEG31 / PWM1.7_A / SPI_MOSI_A
P1.00	I/O	General I/O Port 1.00	PCOM0.0 / SEG0
P1.01	I/O	General I/O Port 1.01	PCOM0.1 / SEG1
P1.02	I/O	General I/O Port 1.02	PCOM0.2 / SEG2
P1.03	I/O	General I/O Port 1.03	PCOM0.3 / SEG3
P1.04	I/O	General I/O Port 1.04	PCOM0.4 / SEG4 / UART2_RxD
P1.05	I/O	General I/O Port 1.05	PCOM0.5 / SEG5 / UART2_TxD
P1.06	I/O	General I/O Port 1.06	PCOM0.6 / SEG6 / Timer2_OVF
P1.07	I/O	General I/O Port 1.07	PCOM0.7 / SEG7 Timer2_T2MX
P1.08	I/O	General I/O Port 1.08	PCOM1.0 / SEG8 / Timer3_EXT
P1.09	I/O	General I/O Port 1.09	PCOM1.1 / SEG9 / Timer4_EXT
P1.10	I/O	General I/O Port 1.10	PCOM1.2 / SEG10 / Timer0_EXT
P1.11	I/O	General I/O Port 1.11	PCOM1.3 / SEG11 / Timer0_T0
P1.12	I/O	General I/O Port 1.12	PCOM1.4 / SEG12 / Timer0_T0EX
P1.13	I/O	General I/O Port 1.13	PCOM1.5 / SEG13 / Timer0_OVF
P1.14	I/O	General I/O Port 1.14	PCOM1.6 / SEG14 / Timer2_T2
P1.15	I/O	General I/O Port 1.15	PCOM1.7 / SEG15 / Timer2_T2EX
P0.00	I/O	General I/O Port 0.00	PWM0.0 / SPI_SSB
P0.01	I/O	General I/O Port 0.01	PWM0.1 / SPI_SCK
P0.02	I/O	General I/O Port 0.02	PWM0.2 / SPI_MISO
P0.03	I/O	General I/O Port 0.03	PWM0.3 / SPI_MOSI
P0.04	I/O	General I/O Port 0.04	PWM0.4
P0.05	I/O	General I/O Port 0.05	PWM0.5
P0.06	I/O	General I/O Port 0.06	PWM0.6
P0.07	I/O	General I/O Port 0.07	PWM0.7
P0.08	I/O	General I/O Port 0.08	PWM1.0
P0.09	I/O	General I/O Port 0.09	PWM1.1
P0.10	I/O	General I/O Port 0.10	PWM1.2
P0.11	I/O	General I/O Port 0.11	PWM1.3
P0.12	I/O	General I/O Port 0.12	PWM1.4
P0.13	I/O	General I/O Port 0.13	PWM1.5
P0.14	I/O	General I/O Port 0.14	PWM1.6
P0.15	I/O	General I/O Port 0.15	PWM1.7

5 Absolute Maximum Ratings

. Absolute Maximum Ratings (TA = 25 °C)

Item	Conditions	Range
DC Voltage in V_{DDIO} relative to Ground	-	-0.5 V to +5.5V
DC Input Voltage	-	-0.5V to (V_{DDIO}+0.5V)
DC Output Voltage	-	-0.5 V to (V_{DDIO}+0.5V)
DC Output Current High	One I/O pin active	-25mA
	All I/O pin active	-100mA
DC Output Current Low	One I/O pin active	+30mA
	All I/O pin active	+150mA
Storage Temperature	-	-65 °C to +150 °C
Soldering Temperature	-	260 °C for 10 seconds

. Recommended Operating Conditions

Item	Symbol		Range
Operating Voltage	V_{DDIO}	Main Power	+2.35V to +5.5V
	V_{DDHOST}	Communication Power	+1.80V to +5.5V
	V_{DDA}	Analog Power	+2.35V to +5.5V
Operating Temperature	-	-	-40℃ to + 85℃

6 DC Characteristics

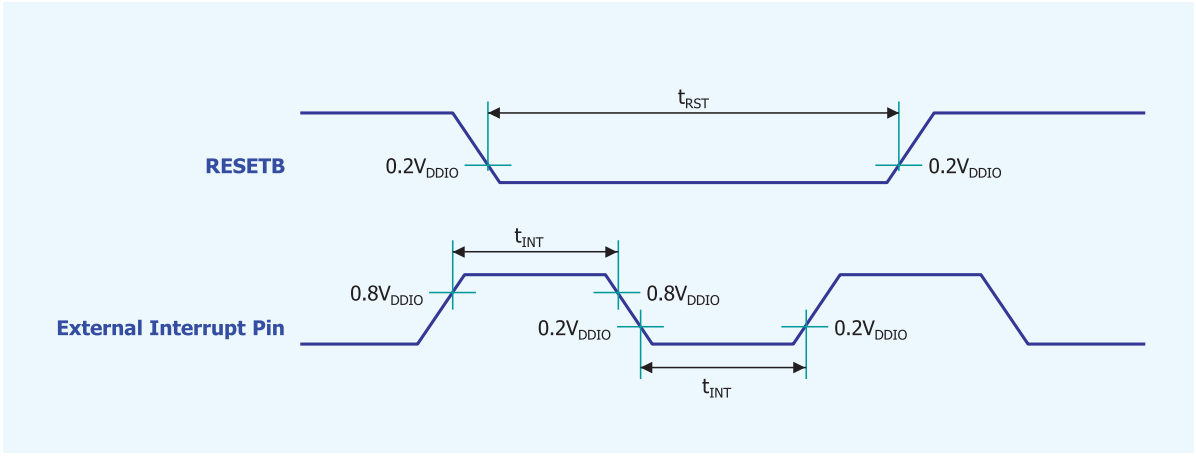
* T_A= -40°C ~ +85°C, V_{DDIO}=2.35V ~ 5.0V unless otherwise specified

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Input Low Voltage	V_{IL}	P0 ~ P5 (Except P5.3, P5.4)	V_{DDIO} = +2.35V to +5.5V	-0.5	-	$0.2V_{DDIO}$ +0.1	V
		P5.3, P5.4	V_{DDIO} = +2.35V to +5.5V	-0.5	-	$0.3V_{DDIO}$	V
Input high Voltage	V_{IH}	P0 ~ P5 (Except P5.3, P5.4)	V_{DDIO} = +2.35V to +5.5V	$0.2V_{DDIO}$ +1.0	-	V_{DDIO} +0.5	V
		P5.3, P5.4	V_{DDIO} = +2.35V to +5.5V	$0.9V_{DDIO}$	-	V_{DDIO} +0.5	
Output Low Voltage	V_{OL}	P0 ~ P5	V_{DDIO} = +3.3V (I_{OL} = 10mA)	-	-	$0.3V_{DDIO}$	V
		P0 ~ P5 (High Current Drive)	V_{DDIO} = +3.3V (I_{OL} = 35mA)	-	-	$0.3V_{DDIO}$	V
Output High Voltage	V_{OH}	P0 ~ P5	V_{DDIO} = +3.3V (I_{OH} = 8mA)	$0.7V_{DDIO}$	-	-	V
Pull-up Resistor	R_{Pu}	P0 ~ P5	V_{DDIO} = +5.0V V_{DDIO} = + 3.3V		37.5 45		KΩ
Crystal Oscillator (System clock)	F_{CRY}	P5.5, P5.6	V_{DDIO} = +2.5V to +5.0V		24		MHz
	T_{WAIT}	P5.5, P5.6	V_{DDIO} = +2.5V to +5.0V	350			us
Crystal Oscillator (Low power clock)	F_{CRY}	P5.3, P5.4	V_{DDIO} = +2.5V to +5.0V		32		KHz
	T_{WAIT}	P5.3, P5.4	V_{DDIO} = +2.5V to +5.0V	200			ms
Logical 1 to 0 Transition Current	I_{TL}	P0 ~ P5	V_{DDIO} = 5.0V±10%	-	500	-	µA
Input Leakage Current	I_{IL}	P0 ~ P5	V_{IN} = V_{IH} or V_{IL}	-	-	±1	µA
Pin Capacitance	C_{IO}	All	V_{DDIO} = +5.0V	-	10	-	pF
Active Current	I_{DD}	V_{SS}	V_{DDIO} = +5.0V POSC=24MHz	-	4	-	mA
Sleep Current	I_{SB}	V_{SS}	V_{DDIO} = +2.35V, T_A=25°C, no I/O sourcing current	-	5	-	µA

7 AC Characteristics

* T_A = -40 ºC ~ +85 ºC, V_{DDIO} = 2.35V ~ 5.0V unless otherwise specified

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
RESETB Input Width	t_{RST}	RESETB	V_{DDIO} = 3V ± 10%	24	-	-	F_{SYS}
External Interrupt Input Width	t_{INT}	External Interrupt	V_{DDIO} = 3V ± 10%	4	-	-	F_{SYS}



8 Analog IP Characteristics

8.1 ADC Characteristics

* TA= -40°C ~ +85°C, V_{DDIO}=2.35V ~ 5.5V unless otherwise specified

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	V_{DDA}	-	2.35	-	5.5	V
Input Voltage	V_{INADC}	-	V_{SS}	-	V_{DDA}	V
Resolution	RES_{ADC}	-	-	12	-	bit
Operating Frequency	F_{ADC}	4.5V < V_{DDA} 2.4V < V_{DDA} ≤ 4.5V 2.35V < V_{DDA} ≤ 2.4V V_{DDA} ≤ 2.35V	-	-	24 12 6 3	MHz
Conversion Time	t_{ADC}	-	-	120 / F_{ADC}	-	Sec
Overall Accuracy	OA_{ADC}	V_{DDA} = 5.0V, F_{ADC} = 24MHz V_{DDA} = 3.3V, F_{ADC} = 12MHz V_{DDA} = 2.4V, F_{ADC} = 6MHz V_{DDA} = 2.35V, F_{ADC} = 3MHz	-	±2	±4	LSB
Integral Nonlinearity	INL_{ADC}		-	±2	±4	LSB
Differential Nonlinearity	DNL_{ADC}		-	±0.5	±1	LSB
Zero Input Error	ZIE_{ADC}		-	±2	±4	LSB
Full Scale Error	FSE_{ADC}		-	±2	±4	LSB
Analog Input Capacitance	CIN_{ADC}	-	-	10	15	pF
Effective Number of Bits	ENOB	2.4V ≤ V_{DDA} ≤ 5.0V	9.9	-	-	BIT
ADC Active Current	I_{ADC}	V_{DDA} = 5.0V, F_{ADC} = 24MHz	-	2.3	3.7	mA
		V_{DDA} = 3.3V, F_{ADC} = 12MHz	-	0.80	1.30	
		V_{DDA} = 2.4V, F_{ADC} = 6MHz	-	0.26	0.46	
		V_{DDA} = 2.35V, F_{ADC} = 3MHz	-	0.18	0.31	

8.2 Comparator Characteristics

* T_A = -40 ºC ~ +85 ºC, V_{DDIO} = 2.35V ~ 5.5V unless otherwise specified

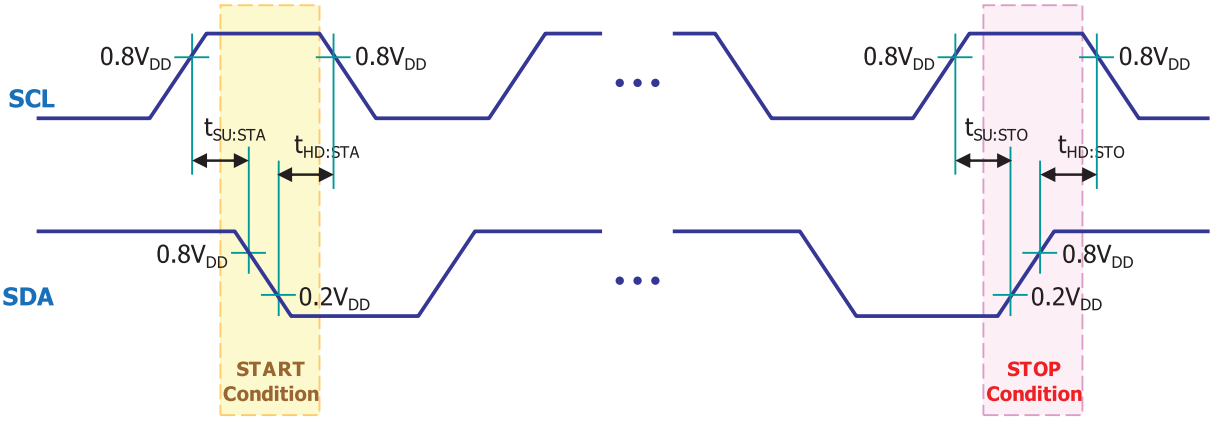
Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Input Offset Voltage	V_{OFFSET_COMP}	V_{DDA} = +2.5V ~ +5.0V	-	10	40	mV
Hysteresis Voltage	V_{Hys_COMP}		-	20	-	mV
Response Time	T_{Rsp_COMP}		-	-	210	ns
Supply Current	I_{ACT_COMP}		-	12	16	uA
Power Down Current	I_{PD_COMP}		-	-	10	nA

8.3 LCD Driver Characteristics

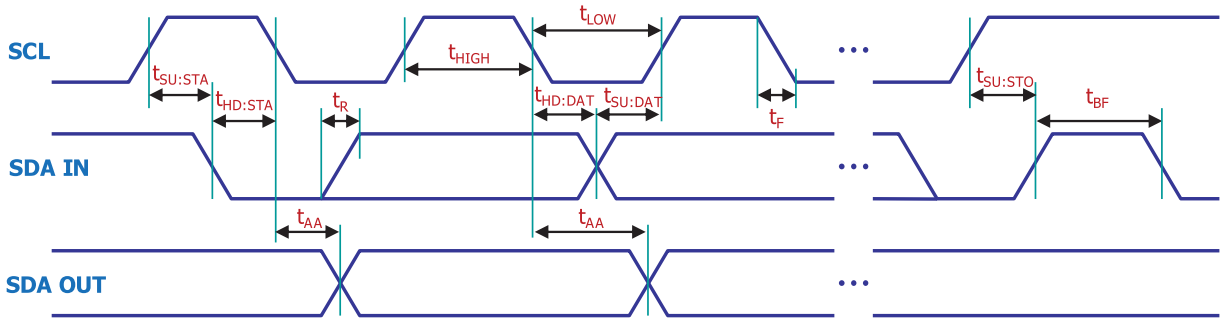
* T_A = -40 ºC ~ +85 ºC, V_{DDIO} = 2.35V ~ 5.5V unless otherwise specified

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
LCD Voltage Driving Resistor	R_{LCD}	V_{LCD3} To V_{SS} Resistance		90		KΩ
LCD Voltage Reference Generation Value	V_{LCD3}	V_{DDIO}@5.0V 1/3Bias, CONTRAST[4:0] = 11000, Or V_{DDIO}@3.3V 1/3Bias, CONTRAST[4:0] = 01000,	3.0	-	-	V
	V_{LCD2}		2.0	-	-	V
	V_{LCD1}		1.0	-	-	V
Supply Current	I_{Sup24}	V_{DDIO} = 2.4V (no load), CONTRAST[4:0] = 01000	-	30	-	uA
	I_{Sup50}	V_{DDIO} = 5.0V (no load), CONTRAST[4:0] = 11000	-	40	-	uA
Output Resistance, COM/SEG	$R_{OCOM/SEG}$	CONTRAST[4:0] = 10000, V_{DDIO}@5.0V	-	-	55	KΩ

9 I2C Timing Characteristics



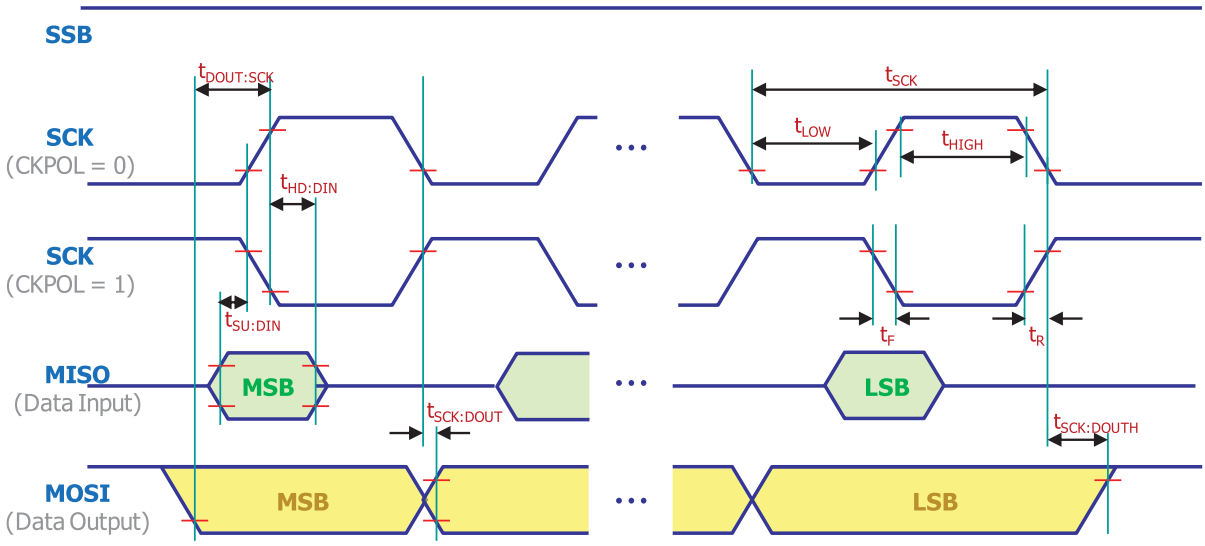
Symbol	Characteristics		Min. [ns]	Max. [ns]	Conditions
$t_{SU:STA}$	START Condition Setup Time	100kHz Mode	4,700	-	Only relevant for repeated START condition
		400kHz Mode	600	-	
$t_{HD:STA}$	START Condition Hold Time	100kHz Mode	4,700	-	After this period, the first clock pulse is generated
		400kHz Mode	600	-	
$t_{SU:STO}$	STOP Condition Setup Time	100kHz Mode	4,700	-	
		400kHz Mode	600	-	
$t_{HD:STO}$	STOP Condition Hold Time	100kHz Mode	4,700	-	
		400kHz Mode	600	-	



Symbol	Characteristics		Min. [ns]	Max. [ns]	Conditions
t_{HIGH}	Clock High Time	100kHz Mode	4,000	-	Minimum Frequency : 1MHz
		400kHz Mode	600	-	Minimum Frequency : 5MHz
t_{LOW}	Clock Low Time	100kHz Mode	4,700	-	Minimum Frequency : 1MHz
		400kHz Mode	1,300	-	Minimum Frequency : 5MHz
$t_{SU:DAT}$	Data Input Setup Time	100kHz Mode	250	-	
		400kHz Mode	100	-	
$t_{HD:DAT}$	Data Input Hold Time	100kHz Mode	0	-	
		400kHz Mode	0	900	
t_{AA}	Data Valid from Clock	100kHz Mode	-	3,500	
		400kHz Mode	-	-	
t_{BF}	BUS Free Time	100kHz Mode	4,700	-	
		400kHz Mode	1,300	-	
t_R	SDA & SCL Rising Time	100kHz Mode	-	1,000	The Range of Cb is from 10pF to 400pF
		400kHz Mode	2.0 + 0.1Cb	300	
t_F	SDA & SCL Falling Time	100kHz Mode	-	300	The Range of Cb is from 10pF to 400pF
		400kHz Mode	2.0 + 0.1Cb	300	

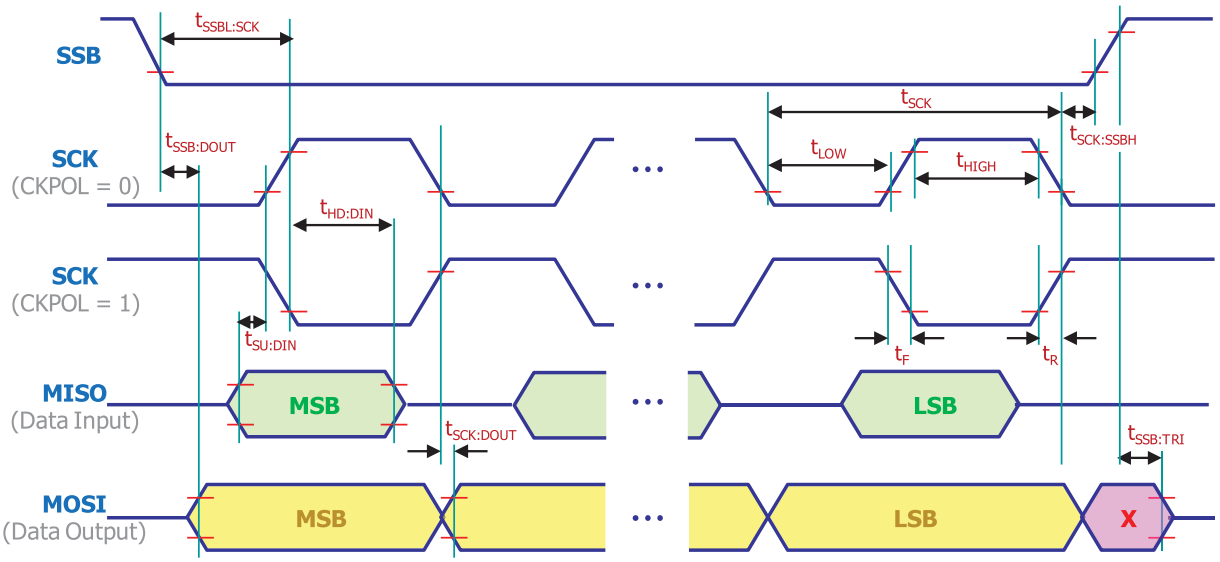
10 SPI Timing Characteristics

10.1 Master Mode



Symbol	Description	Mode	Min. [ns]	Typ. [ns]	Max. [ns]
t_{SCK}	SCK Period Time (using SFR 'SPICK')	Master	-	$F_{OSC}/2$ ~ $F_{OSC}/256$	-
t_{HIGH}, t_{LOW}	SCK High / Low	Master	-	50% Duty Cycle	-
t_F, t_R	SCK Rise / Fall Time	Master	-	3.6	-
$t_{SU:DIN}$	Data Input Setup Time	Master	-	10	-
$t_{HD:DIN}$	Data Input Hold Time	Master	-	10	-
$t_{DOUT:SCK}$	Data Output to SCK	Master	-	0.5 X t_{SCK}	-
$t_{SCK:DOUT}$	SCK to Data Output	Master	-	10	-
$t_{SCK:DOUTH}$	SCK to Data Output High	Master	-	10	-

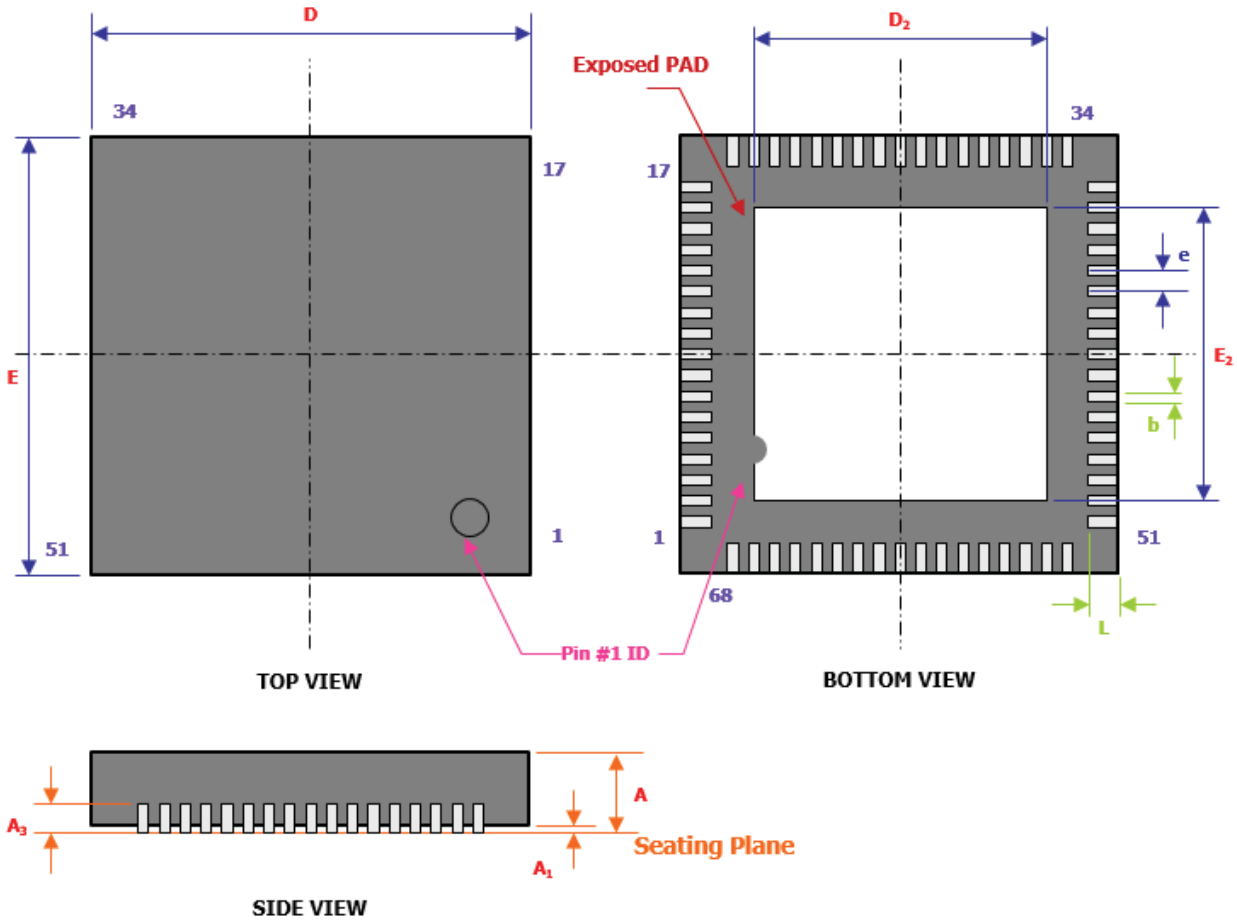
10.2 Slave Mode



Symbol	Description	Mode	Min. [ns]	Typ. [ns]	Max. [ns]
$t_{SSB:DOUT}$	SSB Low to Data Output	Slave	-	15	-
T_{SCK}	SCK Period Time	Slave	4 X t_{Sys}	-	-
t_{HIGH}, t_{LOW}	SCK High / Low	Slave	2 X t_{Sys}	-	-
t_F, t_R	SCK Rise / Fall Time	Slave	-	1,600	-
$t_{SU:DIN}$	Data Input Setup Time	Slave	10	-	-
$t_{HD:DIN}$	Data Input Hold Time	Slave	t_{Sys}	-	-
$t_{SCK:DOUT}$	SCK to Data Output	Slave	-	15	-
$t_{SCK:SSBH}$	SCK to SSB High	Slave	20	-	-
$t_{SSB:TRI}$	SSB High to Tri-state	Slave	-	10	-
$t_{SSBL:SCK}$	SSB Low to SCK	Slave	20	-	-

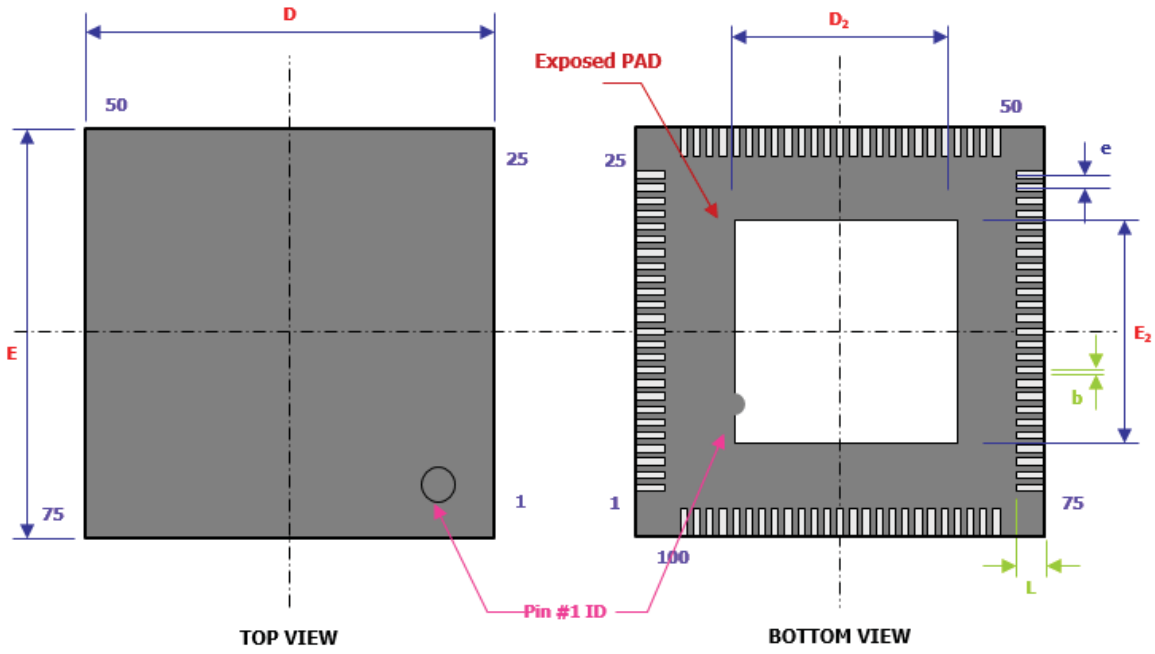
11 Package Dimension

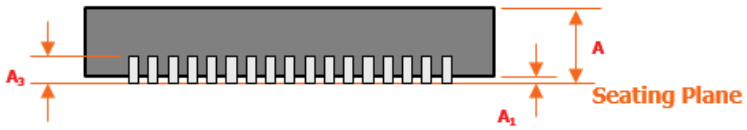
11.1 QFN 68 Pin



Symbol	Dimensions [mm]		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A_1	0.00	0.02	0.03
A_3		0.20	
b	0.15	0.20	0.25
D		8.00	
D_2	4.50	4.60	4.70
E		8.00	
E_2	4.90	5.00	5.10
e		0.40	
L	0.35	0.40	0.45

11.2 QFN 100 Pin





SIDE VIEW

Symbol	Dimensions [mm]		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A_1	0.00	0.02	0.03
A_3		0.20	
b	0.15	0.20	0.25
D		12.00	
D_2	6.80	6.90	7.00
E		12.00	
E_2	6.80	6.90	7.00
e		0.40	
L	0.50	0.60	0.75

12 Revision History

Date	Revision	History
Mar.-2021	0.1	Release
Apr.-2021	0.2	Notation error corrected

MiDAS8000 – QF68IP

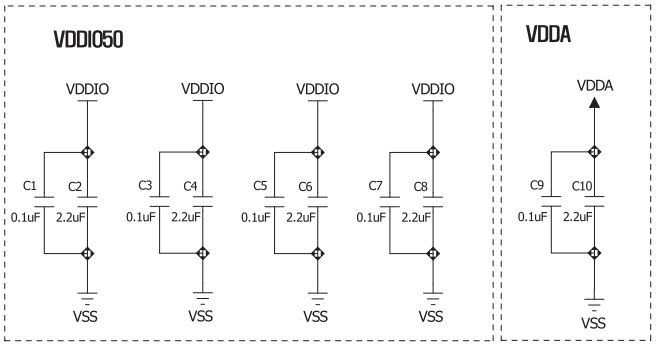
Body Size : 8mm x 8mm

>>VDDIO [Operating Voltage] : +2.35V to +5.5V

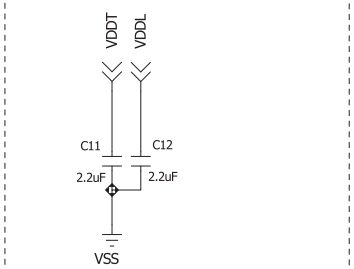
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

* C1 ~ C10 : Mandatory
Power Noise filter Cap

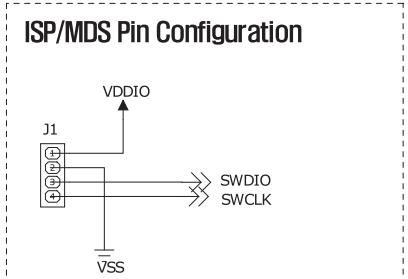
C1, C3, C5, C7, C9 : 0.1uF
C2, C4, C6, C8, C10 : 2.2uF



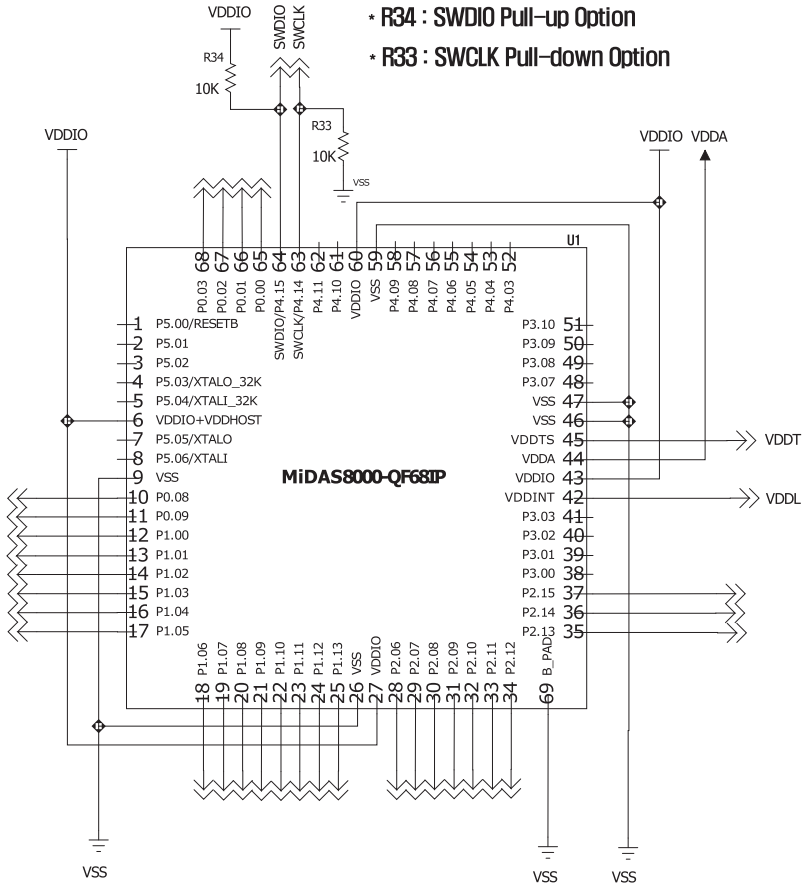
* C11, C12 : Mandatory
LDO Filter Cap
C11 = C12 = 2.2uF



ISP/MDS Pin Configuration



* R34 : SWDIO Pull-up Option
* R33 : SWCLK Pull-down Option



COMPANY:	CORERIVER		
TITLE:	MiDAS8000-QF68IP		
DRAWN: sunhong	DATED: 2020.06.09	CODE: <Code>	SIZE: A2
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: <Drawing Number>	REV: 1.1
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 1 OF 1

MiDAS8000 – QF100IP

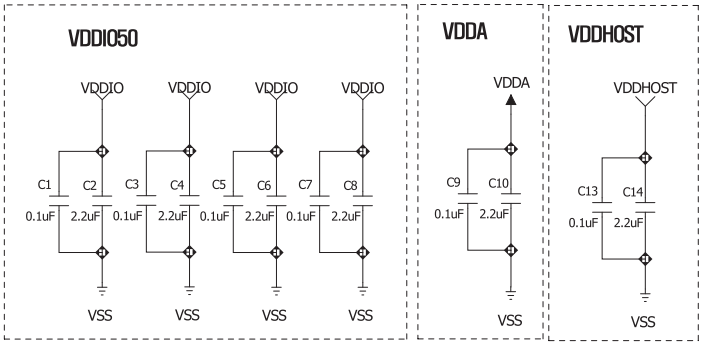
Body Size : 12mm x 12mm

>>VDDIO [Operating Voltage] : +2.35V to +5.5V

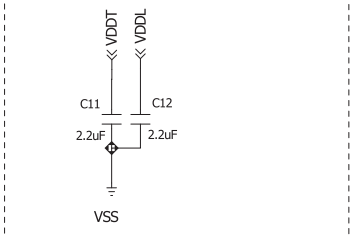
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

* C1 ~ C10 : Mandatory
Power Noise filter Cap

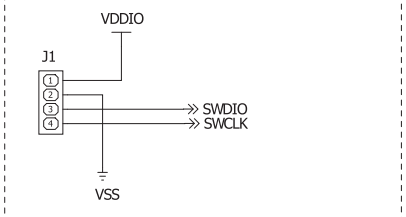
C1, C3, C5, C7, C9, C13 : 0.1uF
C2, C4, C6, C8, C10, C14 : 2.2uF

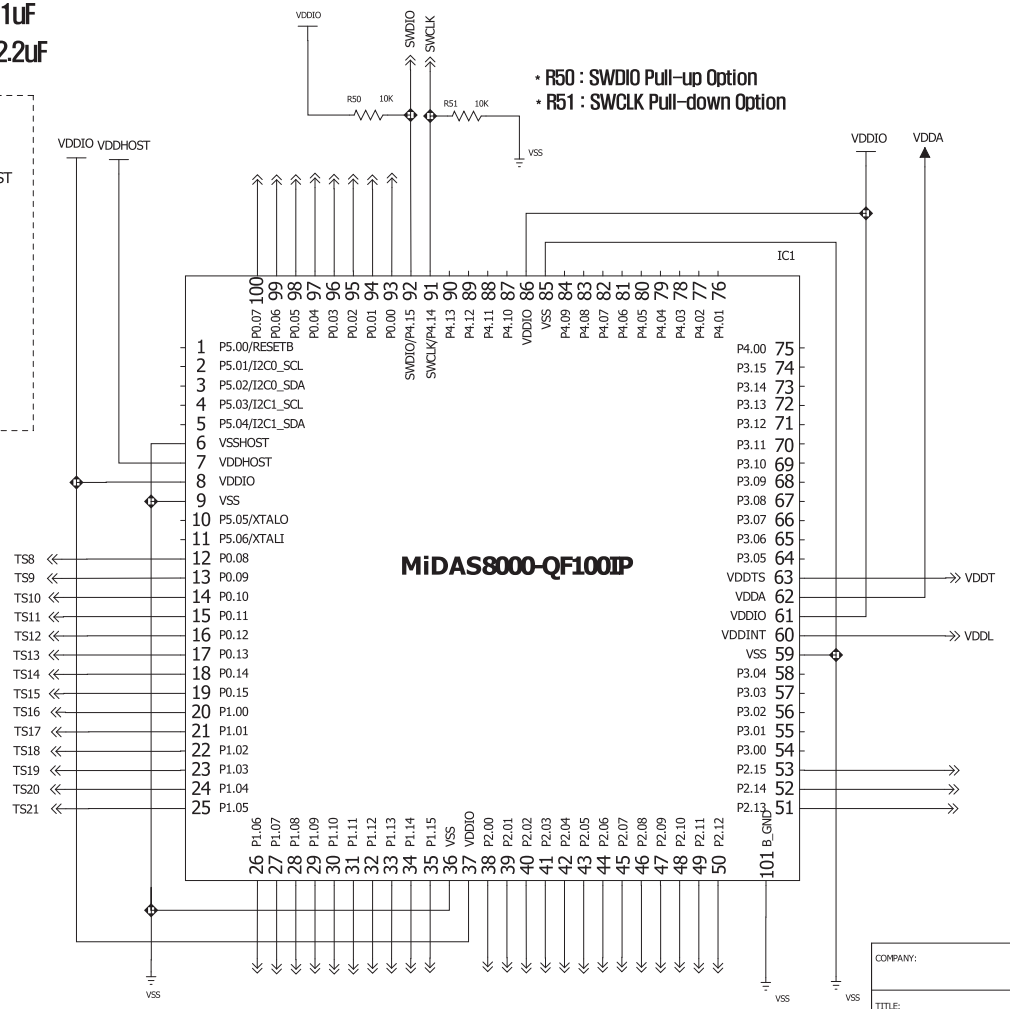


* C11, C12 : Mandatory
LDO Filter Cap
C11 = C12 = 2.2uF



ISP/MDS Pin Configuration





COMPANY: CORERIVER					
TITLE: MiDAS8000-QF100IP					
sunhong	DATED: 2020.06.04				
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: <Code>	SIZE: A2	DRAWING NO: <Drawing Number>	REV: 1.1
QUALITY CONTROL: <QC By>	DATED: <QC Date>				
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 1 OF 1	