CORERIVER
Total Solution of MCU

GC800B

8-Bit Turbo Microcontroller

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1 GC800B Overview

1.1 General Description

The ***GC800B*** of CORERIVER is a group of fast 80C52 compatible microcontrollers. The redesign of its processor core reduces one machine cycle to four system clock cycles. As a result, it executes almost all of its 8052 instructions about 3 times faster than that of traditional 80C52.

GC800B has three timer/counters, maximum 42 programmable I/O pins, maximum 8-channel PWM (Pulse Width Modulator) output, maximum 4 com x 28 segment LCD controller, 1 Watchdog timer, POR (Power-On Reset), 2 UARTs, 1 I2C0(Master/Slave), 1 I2C1(Slave), 1 SPI, maximum 9-channel ADC (Analog to Digital Converter), 1 Comparator, 1 Universal Remote Controller, and 1 LVD (Low Voltage Detector) as peripherals. In addition, it contains an internal precision oscillator and ring oscillator, which can generate the 25 MHz system clock signal instead of a crystal oscillator.

GC800B-QF48EP is qualified to the AEC-Q100 Grade 1 (-40℃ to +125℃), and available in 48-pin QFN package.

On-chip hardware debugging engine help to develop a system. Easy-to-use training kits are also provided.

1.2 Features

- CPU
  - 8-bit turbo 80C52 architecture
  - 4 cycles/ 1 machine cycles
  - Instruction level compatible with Intel 80C52
- 64KB FLASH
- 2KB Internal RAM
  - 1.7KB Internal Aux. RAM
  - 256B Internal RAM
- Operating Voltage: +2.35V to +5.5V
- Operating Frequency
  - Max. 48MHz

- Internal Ring OSC with Calibration function
  - Ring OSC Typ. 25MHz (+/- 3%)
  - Precision OSC Typ. 44.2MHz (+/- 1%)
  - 10KHz (+/- 10%): Low Power OSC.
- Supporting ISP/IAP/MDS
- Three 16/8-bit Timer/Counters
- Two 4-channel High Speed PWMs for LED Dimming
- 24-bit Programmable Watchdog Timer
- 1-channel 12C0 Communication (Master/Slave)
- 1-channel I2C1 Communication (Slave Only)
- 24-bit Sleep Timer
- 1-channel SPI Communication (Master/Slave)
- 2-channel UART Communication
- 9-channel, 12-bit ADC
- Comparator
- Universal Remote Controller
- 4 COM x 28 SEG LCD controller
- 22 Interrupt Sources
  - Timer0/1/2, WDT, SPI, I2C0/1, UART0/2, ADC, PWM0/1
  - COMP / LVD / UR / Sleep Timer
  - 6 External Interrupt
  - Two-level Interrupt Priority
- Reset Sources
  - On-chip Power-On-Reset (POR)
  - External Reset
  - Low Voltage Detector Reset (LVR)
  - Watchdog Timer Reset
- Power Down Wake-up Sources
  - Reset Sources + 6 External Interrupt (Both Levels)
  - Sleep Timer Interrupt
- Power Consumption
  - Active Current : Typ. 1.5mA @5.0V, 4MHz
  - Idle Current : Typ. 700uA @5.0V, 4MHz
  - Stop Current : Typ. 5uA @5.0V

- E.S.D. Protection up to
  - 8,000V for All pin
- Latch-up Protection Up to ±200mA
- Package
  - 48-QFN (6mm X 6mm)

- AEC-Q100 Grade1 (GC800B-QF48EP)

1.3 Applications

- Automotive (AEC-Q100 Grade1, GC800B-QF48EP)
- TV, Monitor, Home Theater
- Refrigerator, Washer, Air conditioner
- Battery power applications

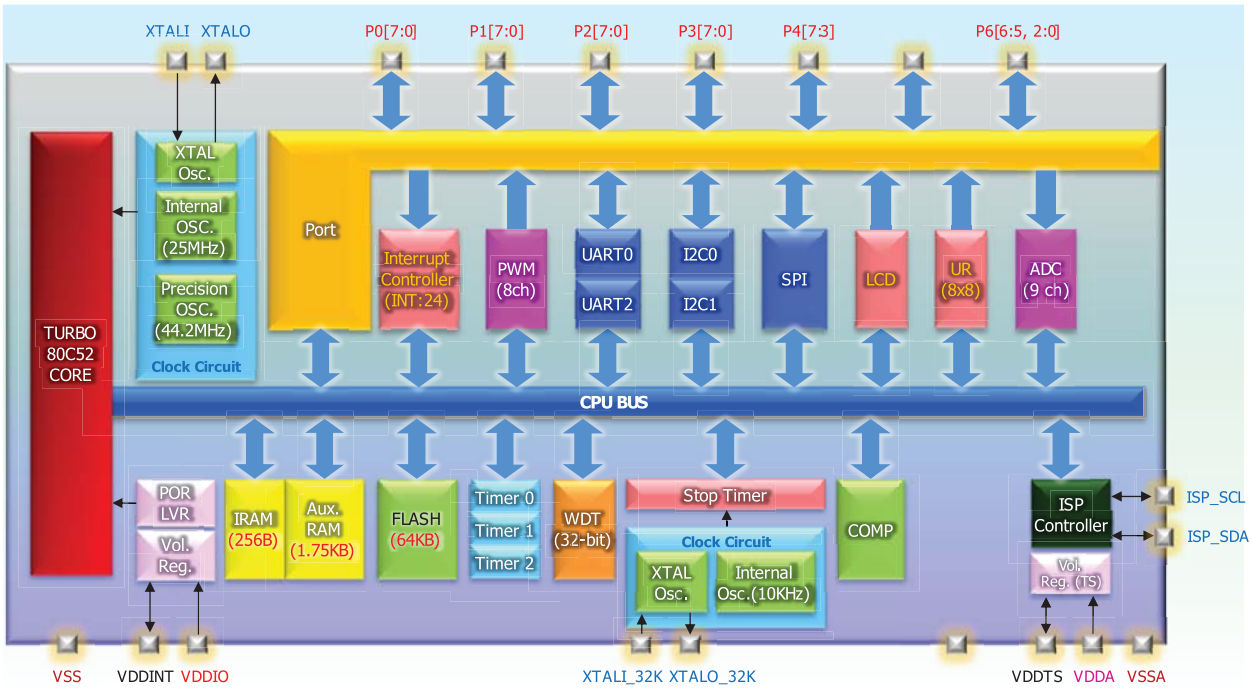
1.4 Product Family Guide

Product	Flash [Byte]	RAM [Byte]	LCD	ADC (bit x Ch)	PWM (bit x Ch)	I/O Pins	Package	Other Peripherals
GC800A-QF68IP	64K	1.7K + 256	4 x 36	12 x 12	8 x 8	56	68-QFN (8x8, 0.85T)	IAP ISP EJTAG 3 T/C 1 I2C 1 SPI 2 UART LCD ADC PWM WDT COMPARATOR LVD POR POSC RING
GC800B-QF48EP (AEC-Q100 Grade 1)	**64K**	**1.7K + 256**	**4 x 28**	**12 x 9**	**8 x 8**	**42**	**48-QFN (6x6, 0.85T)**	
GC800A-QF48IP								
GC801A-QF48IP	64K	1.7K + 256	4 x 26	12 x 9	8 x 8	42	48-QFN (6x6, 0.85T)	

2 Block Diagram

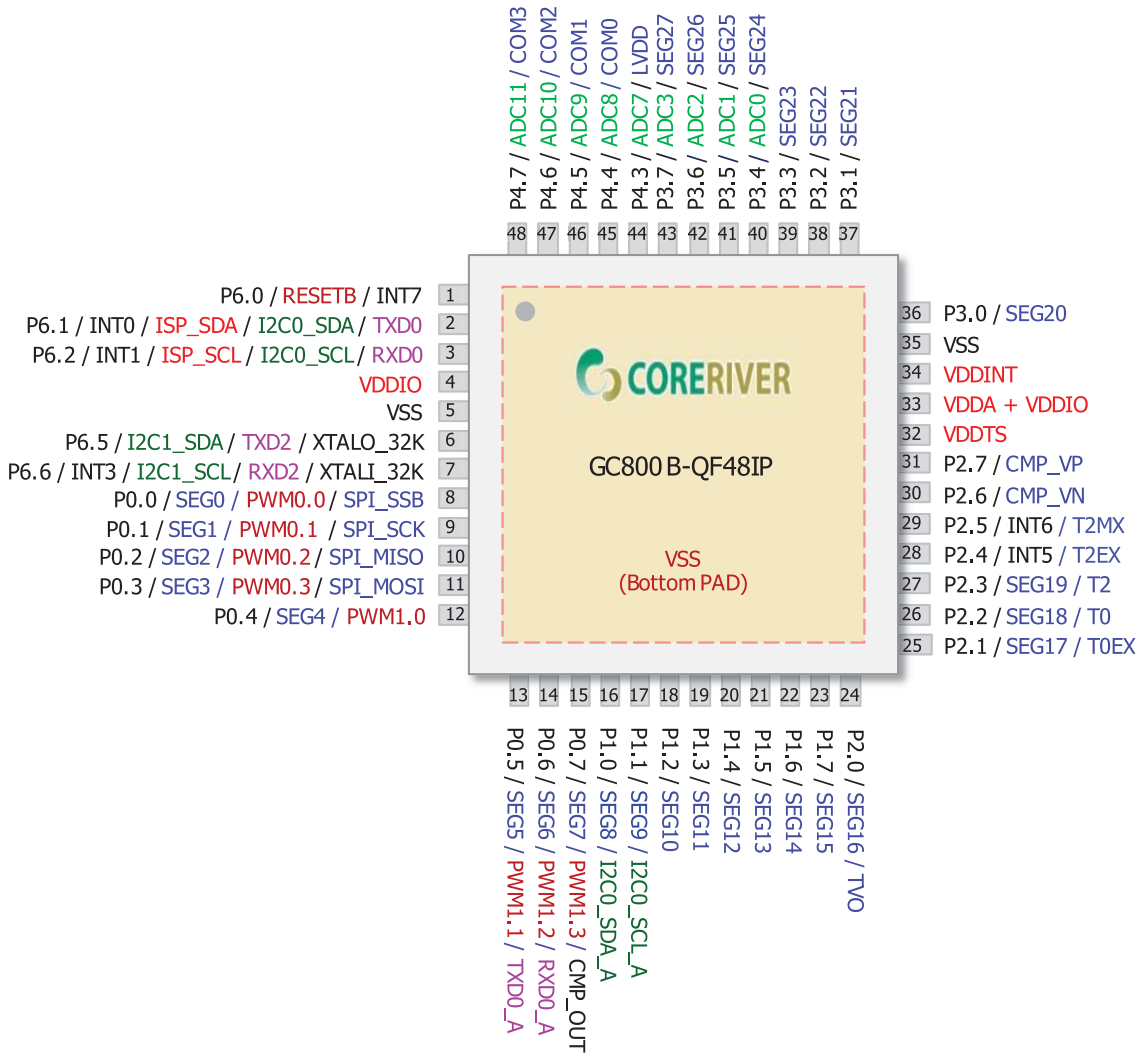
Figure shows the block diagram of ***GC800B***. Programs reside in the internal program memory (Embedded Flash Memory). Data are read from or written to data memory (SRAM) or special function registers (SFRs).

The internal registers of ***GC800B*** are configured as part of the on-chip RAM: therefore each register has an address. This is reasonable for ***GC800B***, since it has so many registers.



3 Pin Configuration

QFN 48 Pin



GC800B-QF48EP Package Diagram

4 Pin Description

GC800B-QF48EP

Pin-No	Symbol	Type	Description	Share Pins
1	P6.0	I/O	General I/O Port 6.0	INT7 / RESETB
2	P6.1	I/O	General I/O Port 6.1	INT0 / ISP_SDA / I2C0_SDA / TxD0
3	P6.2	I/O	General I/O Port 6.2	INT1 / ISP_SCL / I2C0_SCL / RxD0
4	VDDIO	PWR	Power Supply	-
5	VSS	GND	Ground	-
6	P6.5	I/O	General I/O Port 6.5	I2C1_SDA / TxD1 / XTALO_32K
7	P6.6	I/O	General I/O Port 6.6	I2C1_SCL / RxD1 / XTALI_32K / INT3
8	P0.0	I/O	General I/O Port 0.0	SEG0 / PWM0.0 / SPI_SSB
9	P0.1	I/O	General I/O Port 0.1	SEG1 / PWM0.1 / SPI_SCK
10	P0.2	I/O	General I/O Port 0.2	SEG2 / PWM0.2 / SPI_MISO
11	P0.3	I/O	General I/O Port 0.3	SEG3 / PWM0.3 / SPI_MOSI
12	P0.4	I/O	General I/O Port 0.4	SEG4 / PWM1.0 / REM
13	P0.5	I/O	General I/O Port 0.5	SEG5 / PWM1.1 / TxD0_A
14	P0.6	I/O	General I/O Port 0.6	SEG6 / PWM1.2 / RxD0_A
15	P0.7	I/O	General I/O Port 0.7	SEG7 / PWM1.3 / CMP_OUT
16	P1.0	I/O	General I/O Port 1.0	SEG8 / PWM0.0_A / I2C0_SDA_A
17	P1.1	I/O	General I/O Port 1.1	SEG9 / PWM0.1_A / I2C0_SCL_A
18	P1.2	I/O	General I/O Port 1.2	SEG10 / PWM0.2_A
19	P1.3	I/O	General I/O Port 1.3	SEG11 / PWM0.3_A
20	P1.4	I/O	General I/O Port 1.4	SEG12 / PWM1.0_A
21	P1.5	I/O	General I/O Port 1.5	SEG13 / PWM1.1_A
22	P1.6	I/O	General I/O Port 1.6	SEG14 / PWM1.2_A
23	P1.7	I/O	General I/O Port 1.7	SEG15 / PWM1.3_A
24	P2.0	I/O	General I/O Port 2.0	SEG16 / TVO
25	P2.1	I/O	General I/O Port 2.1	SEG17 / T0EX
26	P2.2	I/O	General I/O Port 2.2	SEG18 / T0
27	P2.3	I/O	General I/O Port 2.3	SEG19 / T2
28	P2.4	I/O	General I/O Port 2.4	INT5 / T2EX

29	P2.5	I/O	General I/O Port 2.5	INT6 / T2MX
30	P2.6	I/O	General I/O Port 2.6	CMP_VN
31	P2.7	I/O	General I/O Port 2.7	CMP_VP
32	VDDTS	O	Analog Power Filter	
33	VDDA	PWR	ADC Power Supply	
	VDDIO	PWR	Power Supply	
34	VDDINT	O	Digital Power Filter (+1.5V)	
35	VSS	GND	Ground	
36	P3.0	I/O	General I/O Port 3.0	SEG20
37	P3.1	I/O	General I/O Port 3.1	SEG21
38	P3.2	I/O	General I/O Port 3.2	SEG22
39	P3.3	I/O	General I/O Port 3.3	SEG23
40	P3.4	I/O	General I/O Port 3.4	SEG24 / ADC0
41	P3.5	I/O	General I/O Port 3.5	SEG25 / ADC1
42	P3.6	I/O	General I/O Port 3.6	SEG26 / ADC2
43	P3.7	I/O	General I/O Port 3.7	SEG27 / ADC3
44	P4.3	I/O	General I/O Port 4.3	LVDD / ADC7
45	P4.4	I/O	General I/O Port 4.4	COM0 / ADC8 / I2C1_SDA_A / SPI_SSB_A
46	P4.5	I/O	General I/O Port 4.5	COM1 / ADC9 / I2C1_SCL_A / SPI_SCK_A
47	P4.6	I/O	General I/O Port 4.6	COM2 / ADC10 / TxD2_A / SPI_MISO_A
48	P4.7	I/O	General I/O Port 4.7	COM3 / ADC11 / RxD2_A / SPI_MOSI_A

5 Absolute Maximum Ratings

. Absolute Maximum Ratings (T_A = 25 °C)

Item	Conditions	Range
DC Voltage in V_{DDIO} relative to Ground	-	-0.5 V to +6.0V
DC Input Voltage	-	-0.5V to (V_{DDIO}+0.5V)
DC Output Voltage	-	-0.5 V to (V_{DDIO}+0.5V)
DC Output Current High	One I/O pin active	-25mA
	All I/O pin active	-100mA
DC Output Current Low	One I/O pin active	+30mA
	All I/O pin active	+150mA
Storage Temperature	-	-65 °C to +150 °C
Soldering Temperature	-	260 °C for 10 seconds

. Recommended Operating Conditions

Item	Symbol	Range
Operating Voltage	V_{DDIO}	+2.35V to +5.5V
Operating Temperature (AEC-Q100)	-	-40℃ to + 125℃

6 DC Characteristics

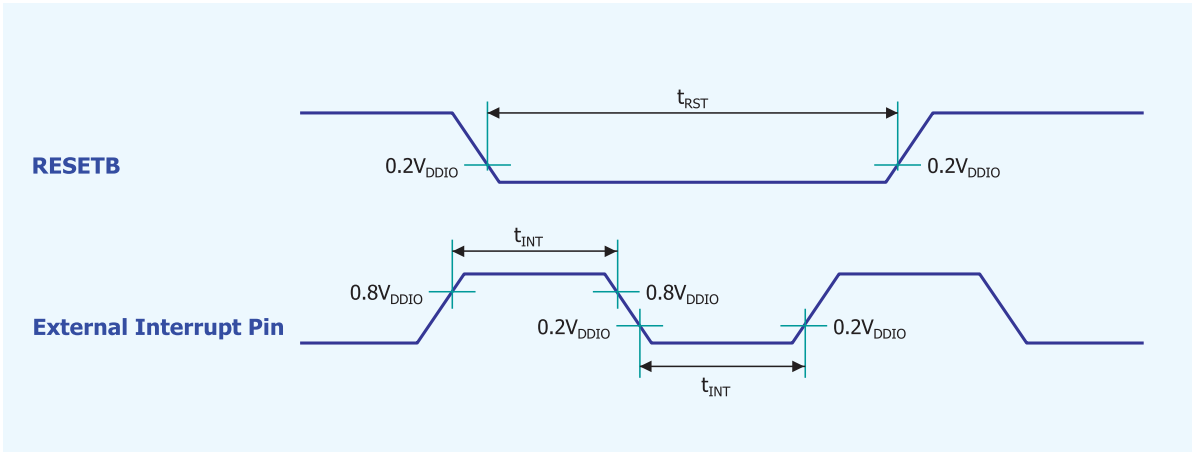
* T_A= -40°C ~ +125°C (AEC-Q100), V_{DDIO}=2.35V ~ 5.5V unless otherwise specified

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Input Low Voltage	V_{IL}	P0 ~ P6 (Except P6.6, P6.5)	V_{DDIO} = +2.35V to +5.5V	-0.5	-	$0.2V_{DDIO}$ +0.1	V
		P6.6, P6.5	V_{DDIO} = +2.35V to +5.5V	-0.5	-	$0.3V_{DDIO}$	V
Input high Voltage	V_{IH}	P0 ~ P6 (Except P6.6, P6.5)	V_{DDIO} = +2.35V to +5.5V	$0.2V_{DDIO}$ +1.0	-	V_{DDIO} +0.5	V
		P6.6, P6.5	V_{DDIO} = +2.35V to +5.5V	$0.9V_{DDIO}$	-	V_{DDIO} +0.5	
Output Low Voltage	V_{OL}	P0 ~ P6	V_{DDIO} = +5.0V (I_{OL} = 8mA) V_{DDIO} = +3.3V (I_{OL} = 4mA)	-	-	$0.3V_{DDIO}$	V
		P0 ~ P6 (High Drive)	V_{DDIO} = +3.3V (I_{OL} = 35mA)	-	-	$0.3V_{DDIO}$	V
Output High Voltage	V_{OH}	P0 ~ P6	V_{DDIO} = +5.0V (I_{OH} = -12mA) V_{DDIO} = +3.3V (I_{OH} = -6mA)	$0.7V_{DDIO}$	-	-	V
Pull-up Resistor	R_{Pu}	P0 ~ P6	V_{DDIO} = +5.5V V_{DDIO} = + 3.3V		37.5 45		KΩ
Logical 1 to 0 Transition Current	I_{TL}	P0 ~ P6	V_{DDIO} = 5.0V±10% (V_{IN} = +1.8V)	-	500	-	μA
Input Leakage Current	I_{IL}	P0 ~ P6	V_{IN} = V_{IH} or V_{IL}	-	-	±1	μA
Pin Capacitance	C_{IO}	All	V_{DDIO} = +5.0V	-	10	-	pF
Active Current	I_{DD}	V_{SS}	V_{DDIO} = +2.35V, T_A=25°C, F_{SYS} =12.5MHz, no I/O sourcing current	-	1.5	-	mA
Sleep Current	I_{SB}	V_{SS}	V_{DDIO} = +2.35V, T_A=25°C, no I/O sourcing current	-	5	-	μA

7 AC Characteristics

* T_A = -40 ºC ~ +125 ºC,(AEC-Q100), V_{DDIO} = 2.35V ~ 5.5V unless otherwise specified

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
RESETB Input Width	t_{RST}	RESETB	V_{DDIO} = 3.0V ± 10%	24	-	-	F_{SYS}
External Interrupt Input Width	t_{INT}	External Interrupt	V_{DDIO} = 3.0V ± 10%	4	-	-	F_{SYS}



8 Analog IP Characteristics

8.1 ADC Characteristics

* T_A= -40°C ~ +125°C (AEC-Q100), V_{DDIO}=2.35V ~ 5.5V unless otherwise specified

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	V_{DDA}	-	2.35	-	5.5	V
Input Voltage	V_{INADC}	-	V_{SS}	-	V_{DDA}	V
Resolution	RES_{ADC}	-	-	12	-	bit
Operating Frequency	F_{ADC}	4.5V < V_{DDA} 2.4V < V_{DDA} ≤ 4.5V 2.35V < V_{DDA} ≤ 2.4V V_{DDA} ≤ 2.35V	-	-	24 12 6 3	MHz
Conversion Time	t_{ADC}	-	-	120 / F_{ADC}	-	Sec
Overall Accuracy	OA_{ADC}	V_{DDA} = 5.0V, F_{ADC} = 24MHz V_{DDA} = 3.3V, F_{ADC} = 12MHz V_{DDA} = 2.4V, F_{ADC} = 6MHz V_{DDA} = 2.35V, F_{ADC} = 3MHz	-	±2	±4	LSB
Integral Nonlinearity	INL_{ADC}		-	±2	±4	LSB
Differential Nonlinearity	DNL_{ADC}		-	±0.5	±1	LSB
Zero Input Error	ZIE_{ADC}		-	±2	±4	LSB
Full Scale Error	FSE_{ADC}		-	±2	±4	LSB
Analog Input Capacitance	CIN_{ADC}	-	-	10	15	pF
Effective Number of Bits	ENOB	2.4V ≤ V_{DDA} ≤ 5.0V	9.9	-	-	BIT
ADC Active Current	I_{ADC}	V_{DDA} = 5.0V, F_{ADC} = 24MHz	-	2.3	3.7	mA
		V_{DDA} = 3.3V, F_{ADC} = 12MHz	-	0.80	1.30	
		V_{DDA} = 2.4V, F_{ADC} = 6MHz	-	0.26	0.46	
		V_{DDA} = 2.35V, F_{ADC} = 3MHz		0.18	0.31	

8.2 Comparator Characteristics

* T_A=-40℃ ~ +125℃ (AEC-Q100)

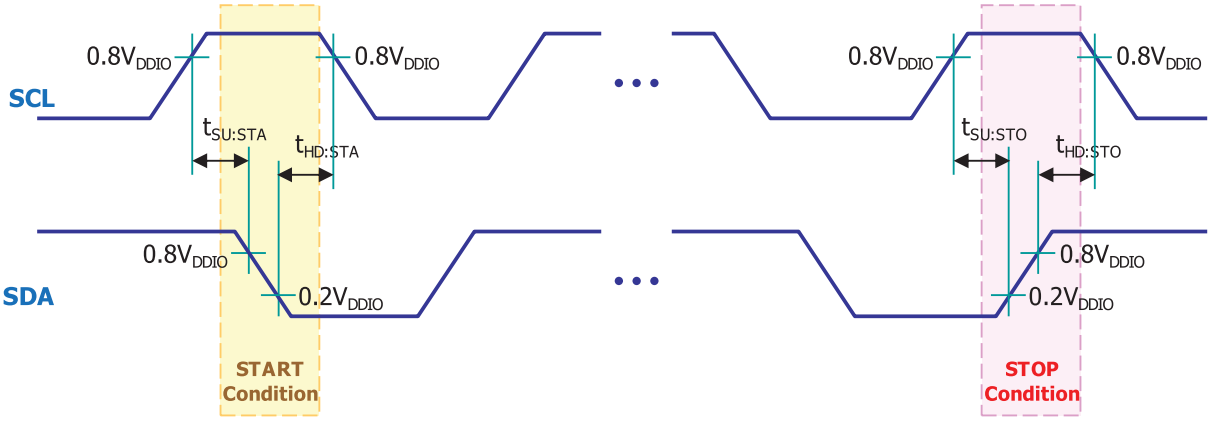
Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Input Offset Voltage	V_{OFFSET_COMP}	V_{DDIO} = +2.5V ~ +5.0V	-	10	40	mV
Hysteresis Voltage	V_{Hys_COMP}		-	20	-	mV
Response Time	T_{Rsp_COMP}		-	-	210	ns
Supply Current	I_{ACT_COMP}		-	12	16	uA
Power Down Current	I_{PD_COMP}		-	-	10	nA

8.3 LCD Driver Characteristics

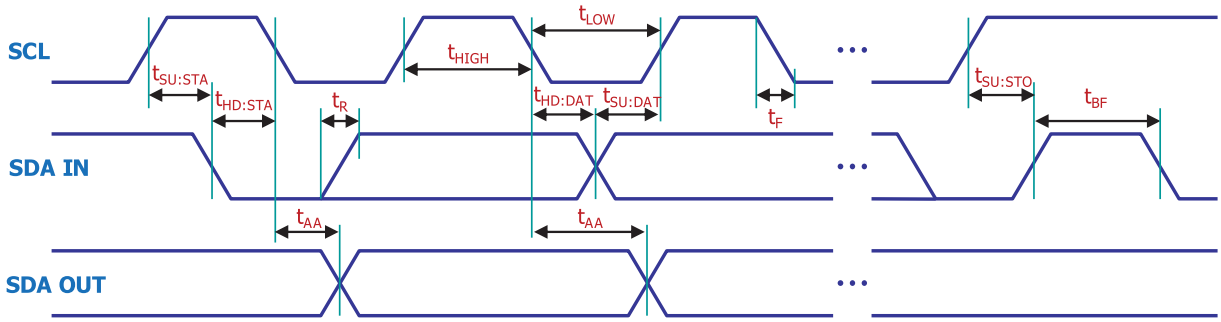
* T_A= -40°C ~ +125°C (AEC-Q100), V_{DDIO}=2.35V ~ 5.5V unless otherwise specified

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
LCD Voltage Driving Resistor	R_{LCD}	V_{LCD3} To V_{SS} Resistance		90		KΩ
LCD Voltage Reference Generation Value	V_{LCD3}	V_{DDIO}@5.0V 1/3Bias, CONTRAST[4:0] = 11000, Or V_{DDIO}@3.3V 1/3Bias, CONTRAST[4:0] = 01000,	3.0	-	-	V
	V_{LCD2}		2.0	-	-	V
	V_{LCD1}		1.0	-	-	V
Supply Current	I_{Sup24}	V_{DDIO} = 2.4V (no load), CONTRAST[4:0] = 01000	-	30	-	uA
	I_{Sup50}	V_{DDIO} = 5.0V (no load), CONTRAST[4:0] = 11000	-	40	-	uA
Output Resistance, COM/SEG	$R_{OCOM/SEG}$	CONTRAST[4:0] = 10000, V_{DDIO}@5.0V	-	-	55	KΩ

9 I2C Timing Characteristics



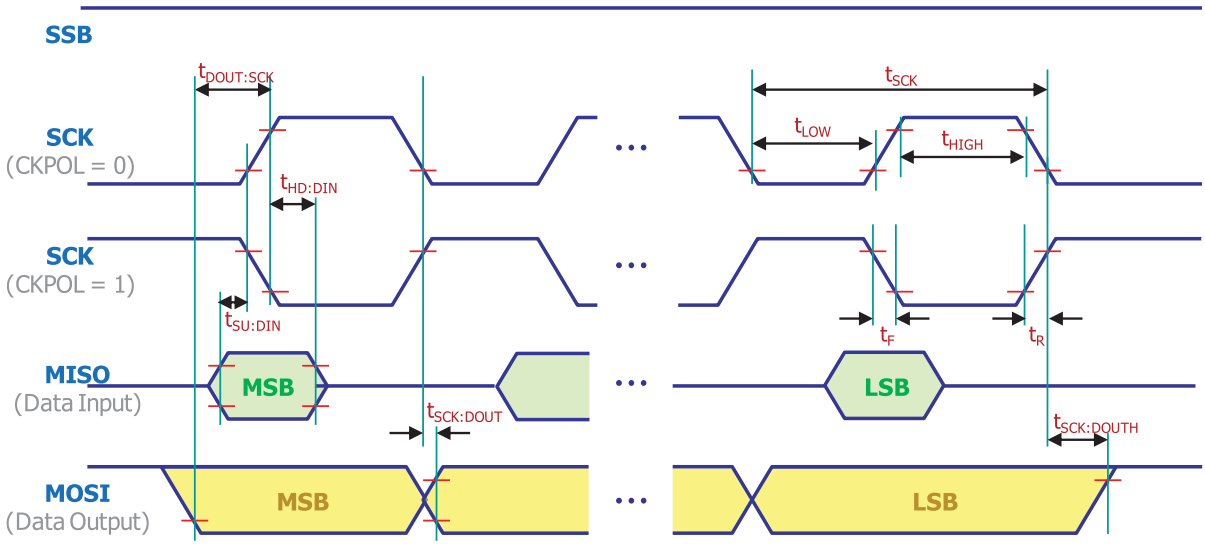
Symbol	Characteristics		Min. [ns]	Max. [ns]	Conditions
$t_{SU:STA}$	START Condition Setup Time	100kHz Mode	4,700	-	Only relevant for repeated START condition
		400kHz Mode	600	-	
$t_{HD:STA}$	START Condition Hold Time	100kHz Mode	4,700	-	After this period, the first clock pulse is generated
		400kHz Mode	600	-	
$t_{SU:STO}$	STOP Condition Setup Time	100kHz Mode	4,700	-	
		400kHz Mode	600	-	
$t_{HD:STO}$	STOP Condition Hold Time	100kHz Mode	4,700	-	
		400kHz Mode	600	-	



Symbol	Characteristics		Min. [ns]	Max. [ns]	Conditions
t_{HIGH}	Clock High Time	100kHz Mode	4,000	-	Minimum Frequency : 1MHz
		400kHz Mode	600	-	Minimum Frequency : 5MHz
t_{LOW}	Clock Low Time	100kHz Mode	4,700	-	Minimum Frequency : 1MHz
		400kHz Mode	1,300	-	Minimum Frequency : 5MHz
$t_{SU:DAT}$	Data Input Setup Time	100kHz Mode	250	-	
		400kHz Mode	100	-	
$t_{HD:DAT}$	Data Input Hold Time	100kHz Mode	0	-	
		400kHz Mode	0	900	
t_{AA}	Data Valid from Clock	100kHz Mode	-	3,500	
		400kHz Mode	-	-	
t_{BF}	BUS Free Time	100kHz Mode	4,700	-	
		400kHz Mode	1,300	-	
t_R	SDA & SCL Rising Time	100kHz Mode	-	1,000	The Range of Cb is from 10pF to 400pF
		400kHz Mode	2.0 + 0.1Cb	300	
t_F	SDA & SCL Falling Time	100kHz Mode	-	300	The Range of Cb is from 10pF to 400pF
		400kHz Mode	2.0 + 0.1Cb	300	

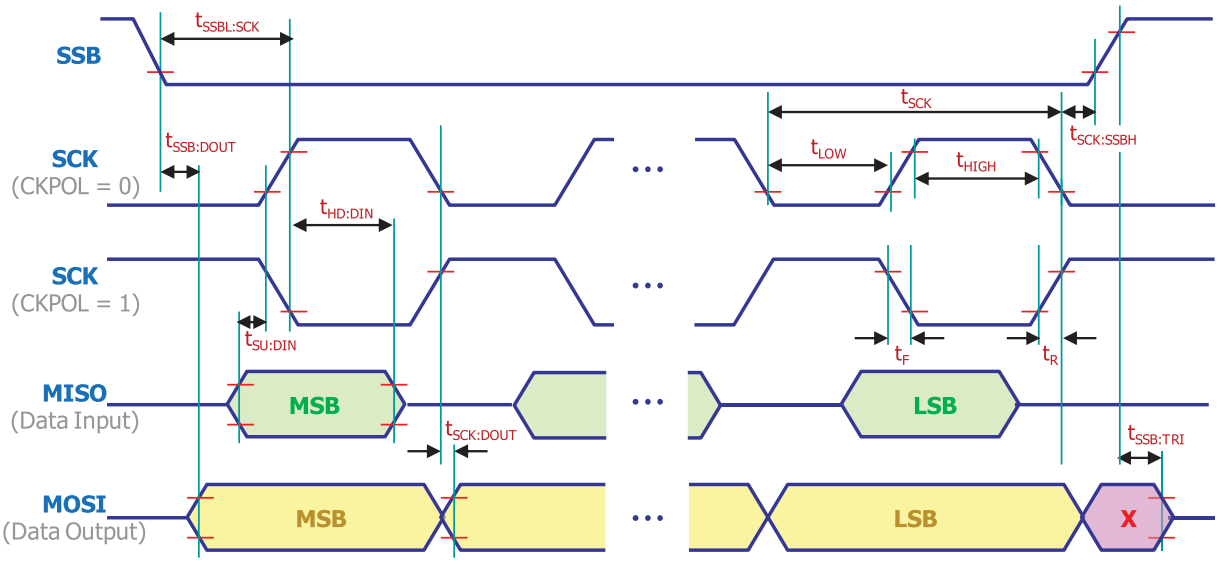
10 SPI Timing Characteristics

10.1 Master Mode



Symbol	Description	Mode	Min. [ns]	Typ. [ns]	Max. [ns]
t_{SCK}	SCK Period Time (using SFR 'SPICK')	Master	-	$F_{OSC}/2$ ~ $F_{OSC}/256$	-
t_{HIGH}, t_{LOW}	SCK High / Low	Master	-	50% Duty Cycle	-
t_F, t_R	SCK Rise / Fall Time	Master	-	3.6	-
$t_{SU:DIN}$	Data Input Setup Time	Master	-	10	-
$t_{HD:DIN}$	Data Input Hold Time	Master	-	10	-
$t_{DOUT:SCK}$	Data Output to SCK	Master	-	0.5 X t_{SCK}	-
$t_{SCK:DOUT}$	SCK to Data Output	Master	-	10	-
$t_{SCK:DOUTH}$	SCK to Data Output High	Master	-	10	-

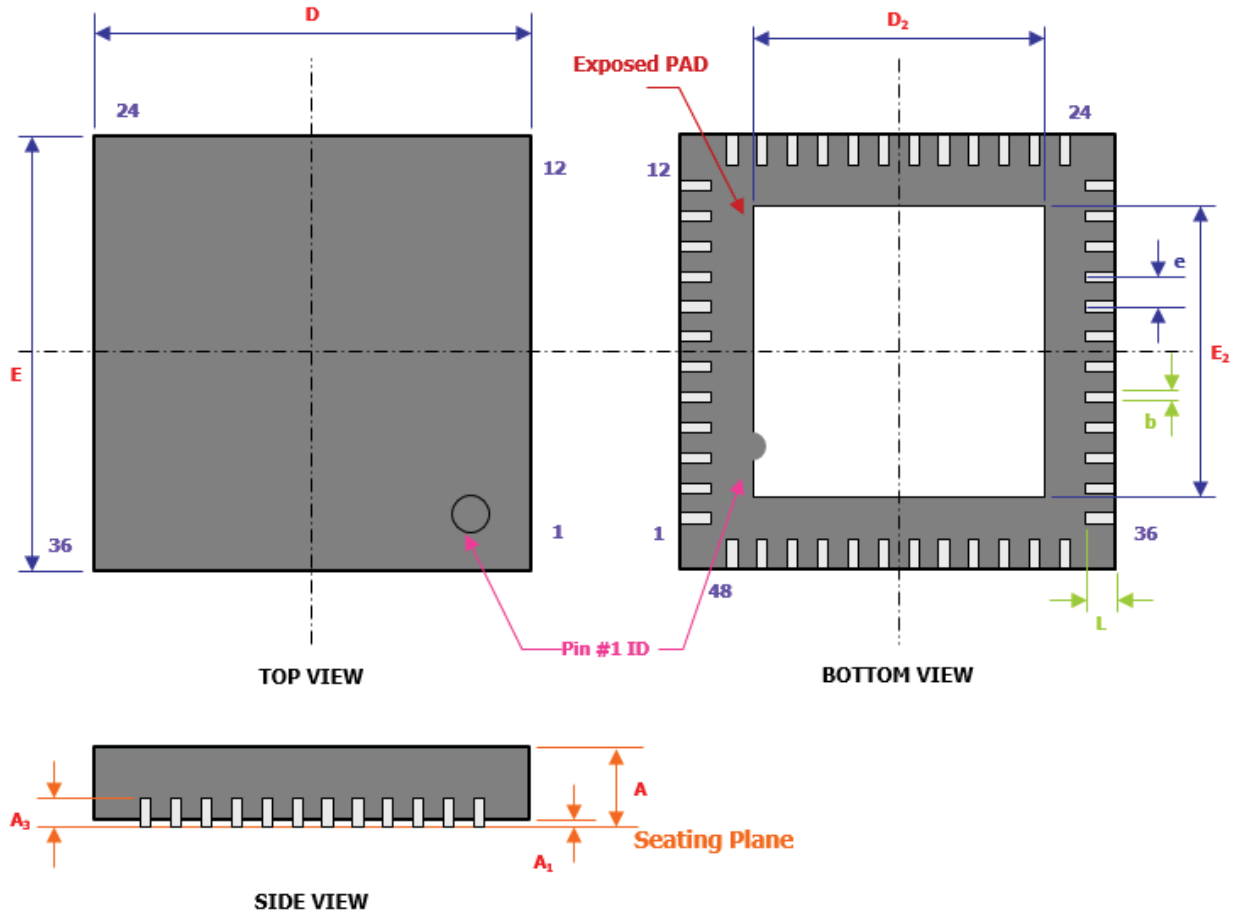
10.2 Slave Mode



Symbol	Description	Mode	Min. [ns]	Typ. [ns]	Max. [ns]
$t_{SSB:DOUT}$	SSB Low to Data Output	Slave	-	15	-
T_{SCK}	SCK Period Time	Slave	4 X t_{Sys}	-	-
t_{HIGH}, t_{LOW}	SCK High / Low	Slave	2 X t_{Sys}	-	-
t_F, t_R	SCK Rise / Fall Time	Slave	-	1,600	-
$t_{SU:DIN}$	Data Input Setup Time	Slave	10	-	-
$t_{HD:DIN}$	Data Input Hold Time	Slave	t_{Sys}	-	-
$t_{SCK:DOUT}$	SCK to Data Output	Slave	-	15	-
$t_{SCK:SSBH}$	SCK to SSB High	Slave	20	-	-
$t_{SSB:TRI}$	SSB High to Tri-state	Slave	-	10	-
$t_{SSBL:SCK}$	SSB Low to SCK	Slave	20	-	-

11 Package Dimension

QFN 48 Pin



Symbol	Dimensions [mm]		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A_1	0.00	0.02	0.03
A_3		0.20	
b	0.15	0.20	0.25
D		6.00	
D_2	4.50	4.60	4.70
E		6.00	
E_2	4.50	4.60	4.70
e		0.40	
L	0.35	0.40	0.45

12 Revision History

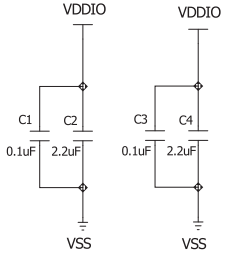
Date	Revision	History
Sep.-2023	1.0	Preliminary release

GC800B – QF48EP

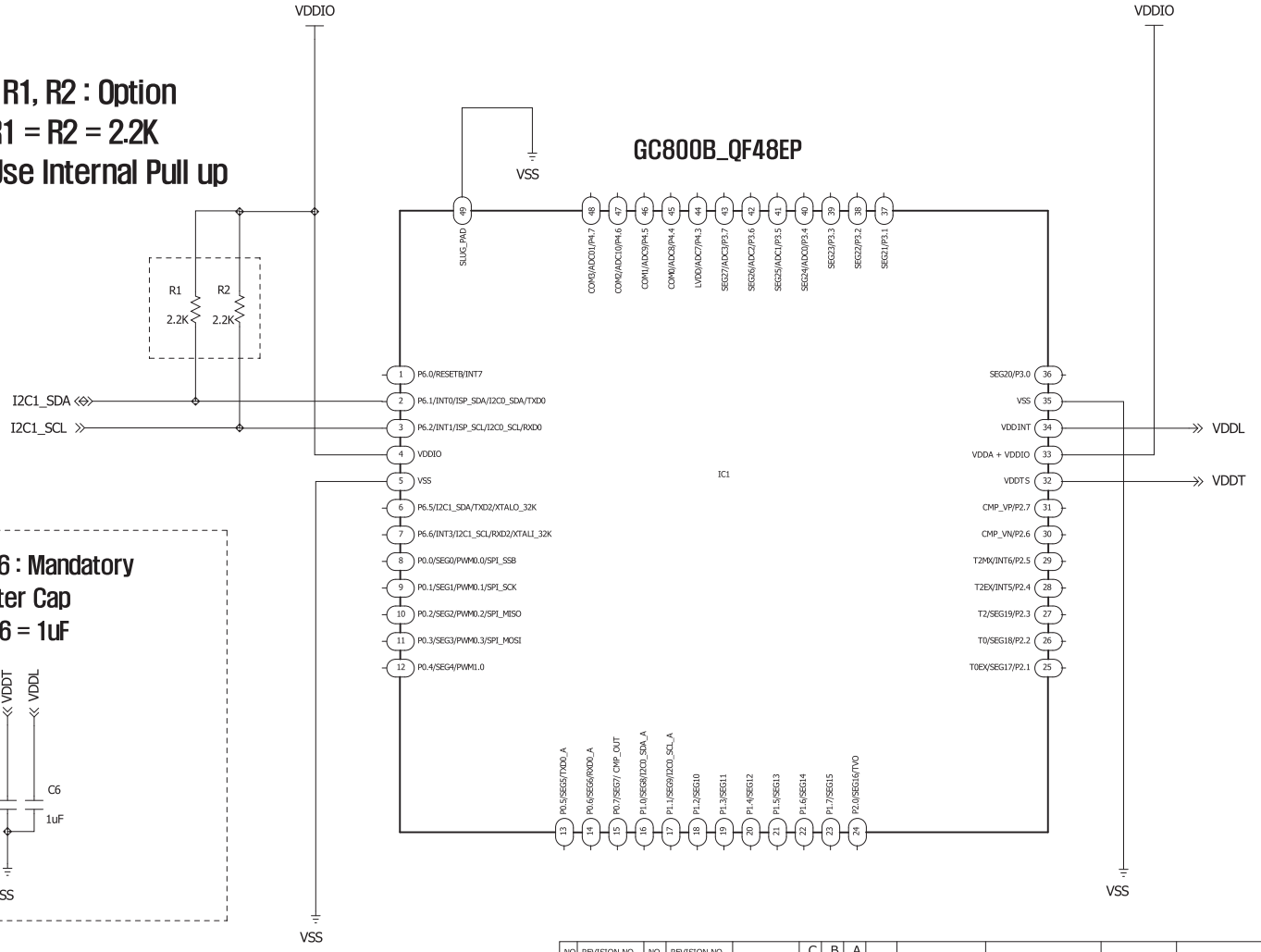
Body Size : 6mm x 6mm

>>VDDIO [Operating Voltage] : +2.35V to +5.5V

* C1 ~ C4 : Mandatory
Power Noise filter Cap
C1, C3 : 0.1uF
C2, C4 : 2.2uF

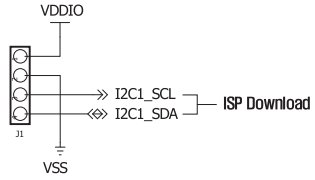


* R1, R2 : Option
R1 = R2 = 2.2K
Use Internal Pull up



* C5, C6 : Mandatory
LDO Filter Cap
C5 = C6 = 1uF

External interface
ISP Download



NO.	REVISION NO.	NO.	REVISION NO.	C B A	NO	PART NO.	DESCRIPTION	METERIAL	COLOR FINISH	NOTE
1				QUANTITY						
2				SCALE A2	UNIT mm	DRAWN. AprilPark	D'SCHEMATIC			
						CHECKD	FILE NAME			
				CORERIVER		APPROVED	GC800B_QF48EP			