CORERIVER
Total Solution of MCU

TouchCore390-QF32IP

Capacitive Touch Screen Controller

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1 TouchCore390-QF32IP Overview

1.1 General Description

TouchCore390-QF32IP is a high-performance Touch Controller for capacitive touch keys. Its engine is an 8-bit 80C51 compatible Processor.

TouchCore390-QF32IP has three timer/counters, maximum 24-channel of touch sensors, maximum 29 programmable I/O pins, 12-channel 8-bit PWMs, Watchdog timer, POR (Power-On Reset), UART, two I2C, SPI, 24-channel 12-bit ADC and LVD (Low Voltage Detector) as peripherals. In addition, it contains an internal ring oscillator, which can generate the 48 MHz system clock signal instead of a crystal oscillator.

TouchCore390-QF32IP has its own architecture for fast sensing. With the hardware filter, it provides noise immunity and excellent sensitivity. The firmware algorithm supports smart sensitivity and compensates for any changes in the sensitivity due to environmental factors such as temperature and humidity.

To effectively manage power, ***TouchCore390-QF32IP*** enables low power consumption by using scan interval and clock control methods after last touch.

TouchCore390-QF32IP operates over the extended -40℃ to +125℃ temperature range, and is available in the 32-pin QFN package.

1.2 Features

- Capacitive touch key controller
  - Supports up to 24 single-type touch keys
  - Supports scroll bar-type touch keys
  - Supports wheel-type touch keys
- Response Time
  - Initial latency of < 20ms for first touch, subject to configuration
  - Programmable frame rate for power saving.
- CPU

- 8-bit Turbo 80C52 Architecture
- 4 Cycles / 1 Machine Cycle
- Instruction Level Compatible with Intel 80C52

◆ Memory
- 32KB Flash (Including 1KB User EEPROM)
- 1KB Internal Aux. RAM
- 256B Internal RAM

◆ Power Supply
- Operating Voltage : +2.7V to +3.6V

◆ Operating Frequency: Max. 48MHz

◆ 29 Programmable I/O Pins

◆ 12-channel 8-bit PWMs

◆ Communication interfaces
- 2-channel I2C Communication
- 1-channel UART Communication
- 1-channel SPI Communication

◆ 24-channel 12-bit ADC

◆ Internal Ring OSC with Calibration function

◆ Supporting ISP/IAP/MDS

◆ 10 Internal Interrupt Sources and 5 External Interrupt Sources

◆ 4 Reset Sources

◆ Power Down Wake-up Sources
- Reset Sources + 5 External Interrupt (Both Levels)
- Watchdog Timer Interrupt

◆ 3 operating modes : Active, Sleep, Deep Sleep

◆ E.S.D. Protection up to
- 8,000V

◆ Latch-up Protection Up to ±200mA

◆ Package
- 32-QFN: 5mm X 5 mm, 0.85T

1.3 Applications

- Home appliance: TV, Monitor, Home Theater
- Mobile Phones
- Portable MP3, MP4
- Digital Cameras
- Battery power applications

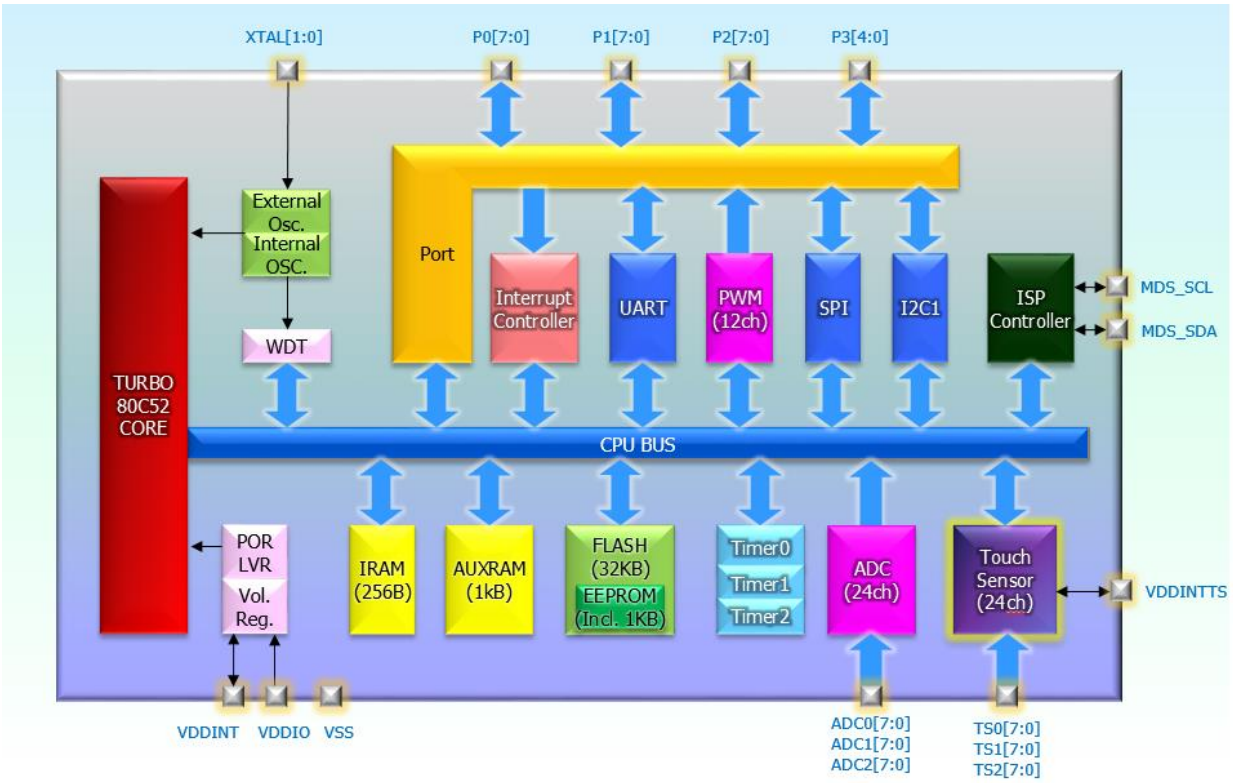
1.4 Product Family Guide

Product	Touch Channels	Flash [Byte]	Package
TouchCore320-ML16IP	2	8K	4 x 4 mm, 0.85T, 16-pin MLF
TouchCore350-TS20IP	8	8K	20-pin TSSOP
TouchCore350-QF16IP	8	8K	3 x 3 mm, 0.85T, 16-pin QFN
TouchCore350-ML16IP	8	8K	4 x 4mm, 0.85T, 16-pin MLF
TouchCore351-ML16IP	8	8K	4 x 4 mm, 0.85T, 16-pin MLF
TouchCore360-QF16IP	7	12K	3 x 3 mm, 0.55T, 16-pin QFN
TouchCore370-ML24IP	8	12K	4 x 4 mm, 0.85T, 24-pin MLF
TouchCore371-ML24IP	8	12K	4 x 4 mm, 0.85T, 24-pin MLF
TouchCore380-TS28IP	16	16K	28-pin TSSOP
TouchCore380-SO28IP	16	16K	28-pin SOP
TouchCore380-ML24IP	16	16K	4 x 4 mm, 0.85T, 24-pin MLF
TouchCore390-ML32IP	16	32K	5 x 5 mm, 0.85T, 32-pin MLF
TouchCore390-QF32IP	**24**	**32K**	**5 x 5 mm, 0.85T, 32-pin QFN**

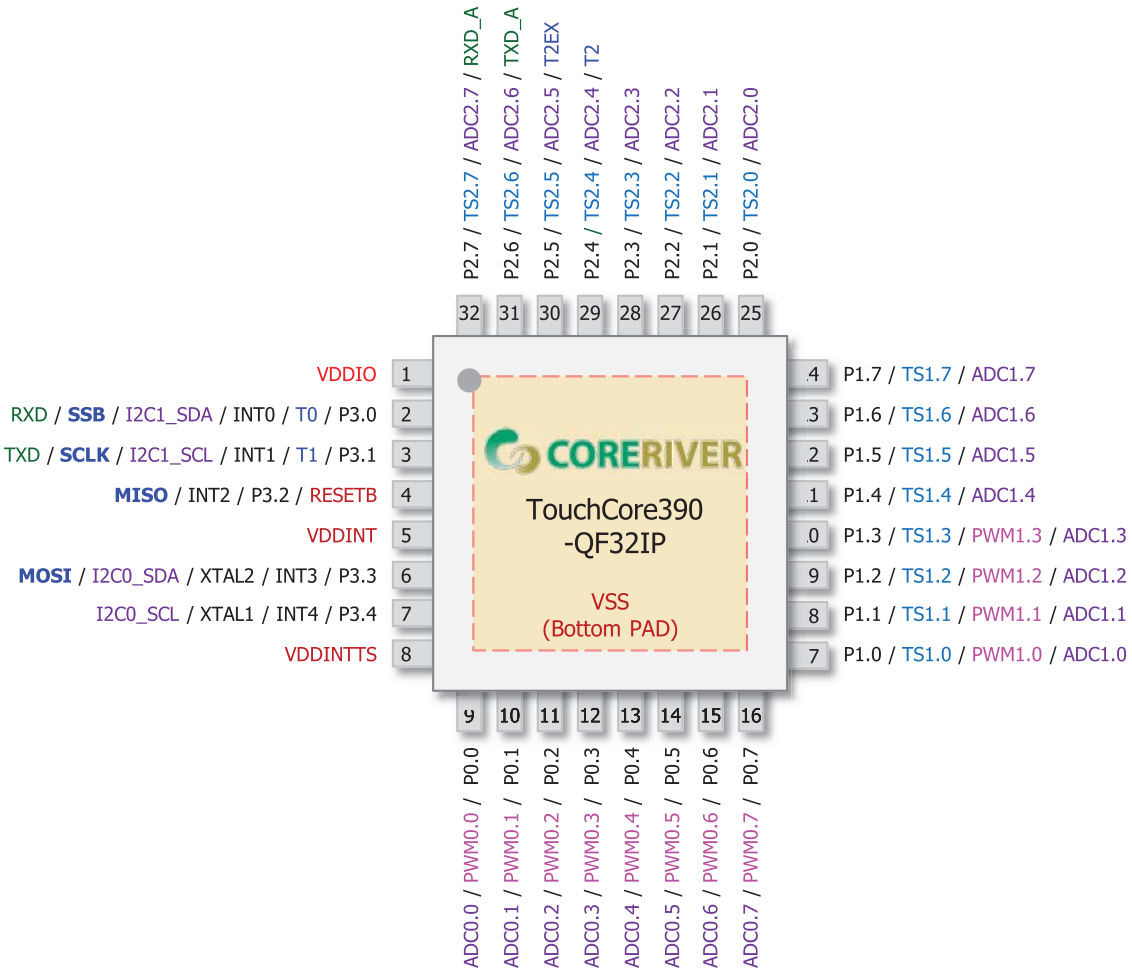
2 Block Diagram

Figure shows the block diagram of ***TouchCore390-QF32IP***. Programs reside in the internal program memory (Embedded Flash Memory). Data are read from or written to data memory (SRAM) or special function registers (SFRs).

The internal registers of ***TouchCore390-QF32IP*** are configured as part of the on-chip RAM: therefore each register has an address. This is reasonable for ***TouchCore390-QF32IP***, since it has so many registers.



3 Pin Configuration



32-pin QFN Package Diagram

4 Pin Description

Pin No.	Name	Type	Description	Share Pins
1	VDDIO	PWR		
2	P3.0	I/O	General I/O Port 3.0	RXD / SSB / I2C1_SDA / INT0 / T0
3	P3.1	I/O	General I/O Port 3.1	TXD / SCLK / I2C1_SCL / INT1 / T1
4	P3.2	I/O	General I/O Port 3.2	INT2 / RESETB / MISO
5	VDDINT	O	Digital Power Filter (+1.8V)	
6	P3.3	I/O	General I/O Port 3.3	INT3 / XTAL2 / I2C0_SDA / MOSI
7	P3.4	I/O	General I/O Port 3.4	INT4 / XTAL1 / I2C0_SCL
8	VDDINTS	O	Touch Sensor Power Filter	
9	TS0.0	I/O	Touch Sensing Channel 0.0	P0.0 / PWM0.0 / ADC0.0
10	TS0.1	I/O	Touch Sensing Channel 0.1	P0.1 / PWM0.1 / ADC0.1
11	TS0.2	I/O	Touch Sensing Channel 0.2	P0.2 / PWM0.2 / ADC0.2
12	TS0.3	I/O	Touch Sensing Channel 0.3	P0.3 / PWM0.3 / ADC0.3
13	TS0.4	I/O	Touch Sensing Channel 0.4	P0.4 / PWM0.4 / ADC0.4
14	TS0.5	I/O	Touch Sensing Channel 0.5	P0.5 / PWM0.5 / ADC0.5
15	TS0.6	I/O	Touch Sensing Channel 0.6	P0.6 / PWM0.6 / ADC0.6
16	TS0.7	I/O	Touch Sensing Channel 0.7	P0.7 / PWM0.7 / ADC0.7
17	TS1.0	I/O	Touch Sensing Channel 1.0	P1.0 / PWM1.0 / ADC1.0
18	TS1.1	I/O	Touch Sensing Channel 1.1	P1.1 / PWM1.1 / ADC1.1
19	TS1.2	I/O	Touch Sensing Channel 1.2	P1.2 / PWM1.2 / ADC1.2
20	TS1.3	I/O	Touch Sensing Channel 1.3	P1.3 / PWM1.3 / ADC1.3
21	TS1.4	I/O	Touch Sensing Channel 1.4	P1.4 / ADC1.4
22	TS1.5	I/O	Touch Sensing Channel 1.5	P1.5 / ADC1.5
23	TS1.6	I/O	Touch Sensing Channel 1.6	P1.6 / ADC1.6
24	TS1.7	I/O	Touch Sensing Channel 1.7	P1.7 / ADC1.7
25	TS2.0	I/O	Touch Sensing Channel 2.0	P2.0 / ADC2.0
26	TS2.1	I/O	Touch Sensing Channel 2.1	P2.1 / ADC2.1
27	TS2.2	I/O	Touch Sensing Channel 2.2	P2.2 / ADC2.2
28	TS2.3	I/O	Touch Sensing Channel 2.3	P2.3 / ADC2.3
29	TS2.4	I/O	Touch Sensing Channel 2.4	P2.4 / ADC2.4 / T2
30	TS2.5	I/O	Touch Sensing Channel 2.5	P2.5 / ADC2.5 / T2EX
31	TS2.6	I/O	Touch Sensing Channel 2.6	P2.6 / ADC2.6 / TXD_A
32	TS2.7	I/O	Touch Sensing Channel 2.7	P2.7 / ADC2.7 / RXD_A

5 Absolute Maximum Ratings

.Absolute Maximum Ratings(TA = 25 °C)

Item	Conditions	Range
DC Voltage in V_{DDIO} relative to Ground	-	-0.5 V to +4.6V
DC Input Voltage	-	-0.5V to (V_{DDIO}+0.5V)
DC Output Voltage	-	-0.5 V to (V_{DDIO}+0.5V)
DC Output Current High	One I/O pin active	-25mA
	All I/O pin active	-100mA
DC Output Current Low	One I/O pin active	+30mA
	All I/O pin active	+150mA
Storage Temperature	-	-65 °C to +150 °C
Soldering Temperature	-	260 °C for 10 seconds

.Recommended Operating Conditions

Item	Conditions	Range
Operating Voltage	-	+2.7 V to +3.6V
Operating Temperature	-	-40℃ to + 125℃

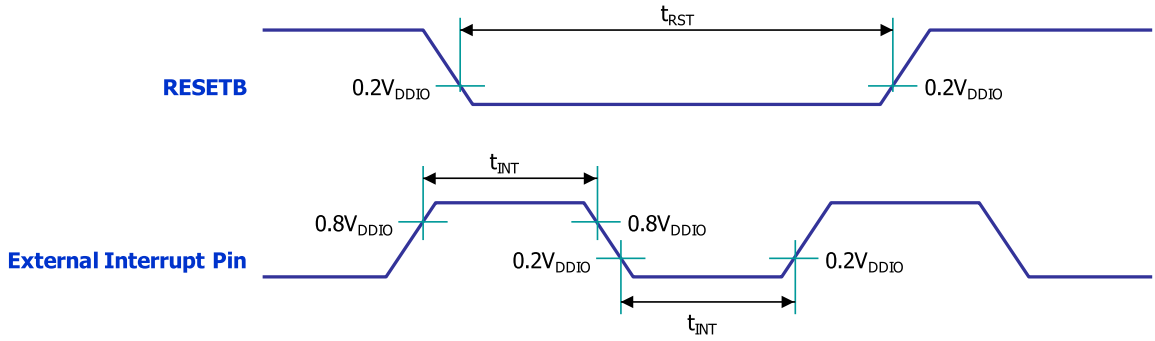
6 DC Characteristics

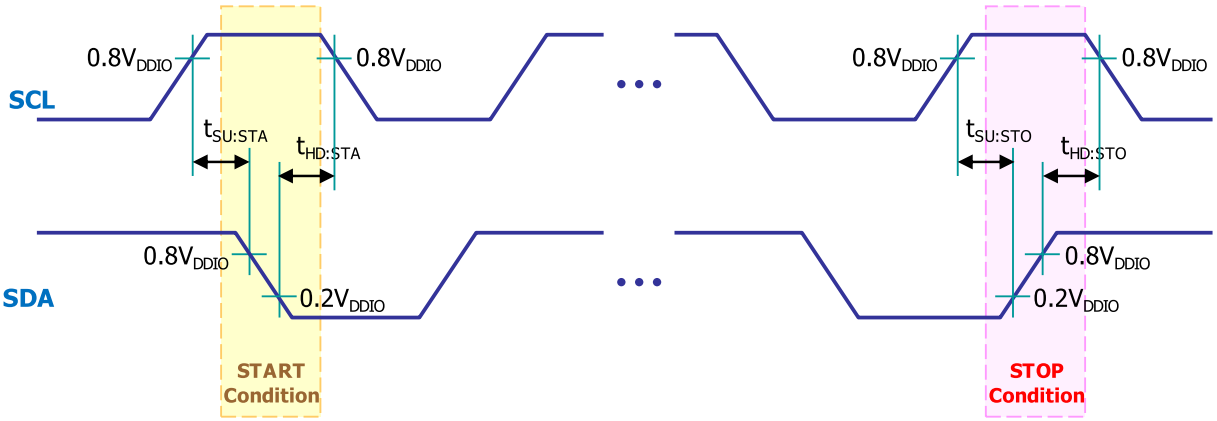
* T_A= -40°C ~ +125°C, V_{DDIO}=2.7V ~ 3.6V unless otherwise specified

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Input Low Voltage	V_{IL}	P0,P1,P2,P3	V_{DDIO} = 2.7V~3.6V	-0.5	-	$0.2V_{DDIO}$ +0.1	V
Input high Voltage	V_{IH}	P0,P1,P2,P3	V_{DDIO} = 2.7V~3.6V	$0.2V_{DDIO}$ +1.0	-	V_{DDIO} +0.5	V
Output Low Voltage	V_{OL}	P0,P1,P2,P3	V_{DDIO} = 3.0V~3.6V (I_{OL} = 4.35mA) V_{DDIO} = 2.7V~3.0V (I_{OL} = 3.55mA)	-	-	$0.3V_{DDIO}$	V
		P0,P1,P2,P3[1:0] (High Drive)	V_{DDIO} = 3.0V~3.6V (I_{OL} = 34.79mA) V_{DDIO} = 2.7V~3.0V (I_{OL} = 28.41mA)	-	-	$0.3V_{DDIO}$	V
Output High Voltage	V_{OH}	P0,P1,P2,P3	V_{DDIO} = 3.0V~3.6V (I_{OH} = -8.04mA) V_{DDIO} = 2.7V~3.0V (I_{OH} = -6.62mA)	$0.7V_{DDIO}$	-	-	V
	V_{OHP}	P0,P1,P2,P3 (Pull-up Resistor Only)	V_{DDIO} = 3.0V~3.6V (I_{OHP} = -30.30uA) V_{DDIO} = 2.7V~3.0V (I_{OHP} = -24.26uA)	$0.7V_{DDIO}$	-	-	V
Logical 1 to 0 Transition Current	I_{TL}	P0,P1,P2,P3	V_{DDIO} = 3.0V±10% (V_{IN}=2V)	-	-	-650	μA
Input Leakage Current	I_{IL}	P0,P1,P2,P3	V_{IN} = V_{IH} or V_{IL}	-	-	± 1	μA
Pin Capacitance	C_{IO}	All	V_{DDIO} = 3.0V	-	10	-	pF

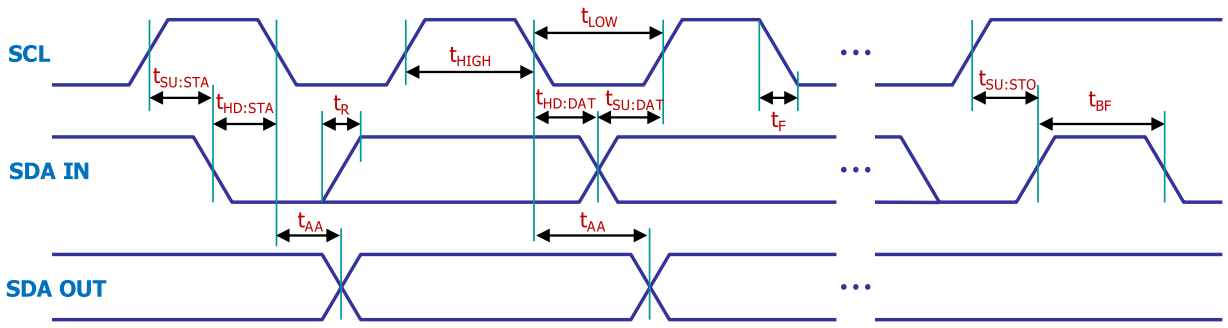
7 AC Characteristics

* T_A = -40 °C ~ +125 °C, V_{DDIO} = 2.7V ~ 3.6V unless otherwise specified



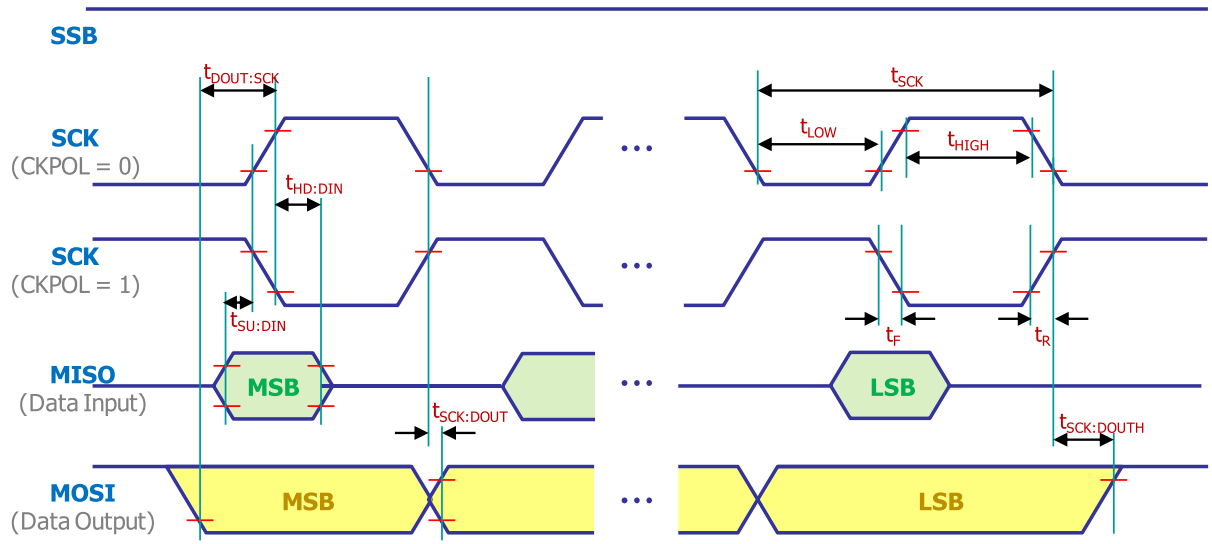


Symbol	Characteristics		Min. [ns]	Max. [ns]	Conditions
$t_{SU:STA}$	START Condition Setup Time	100kHz Mode	4,700	-	Only relevant for repeated START condition
		400kHz Mode	600	-	
$t_{HD:STA}$	START Condition Hold Time	100kHz Mode	4,700	-	After this period, the first clock pulse is generated
		400kHz Mode	600	-	
$t_{SU:STO}$	STOP Condition Setup Time	100kHz Mode	4,700	-	
		400kHz Mode	600	-	
$t_{HD:STO}$	STOP Condition Hold Time	100kHz Mode	4,700	-	
		400kHz Mode	600	-	

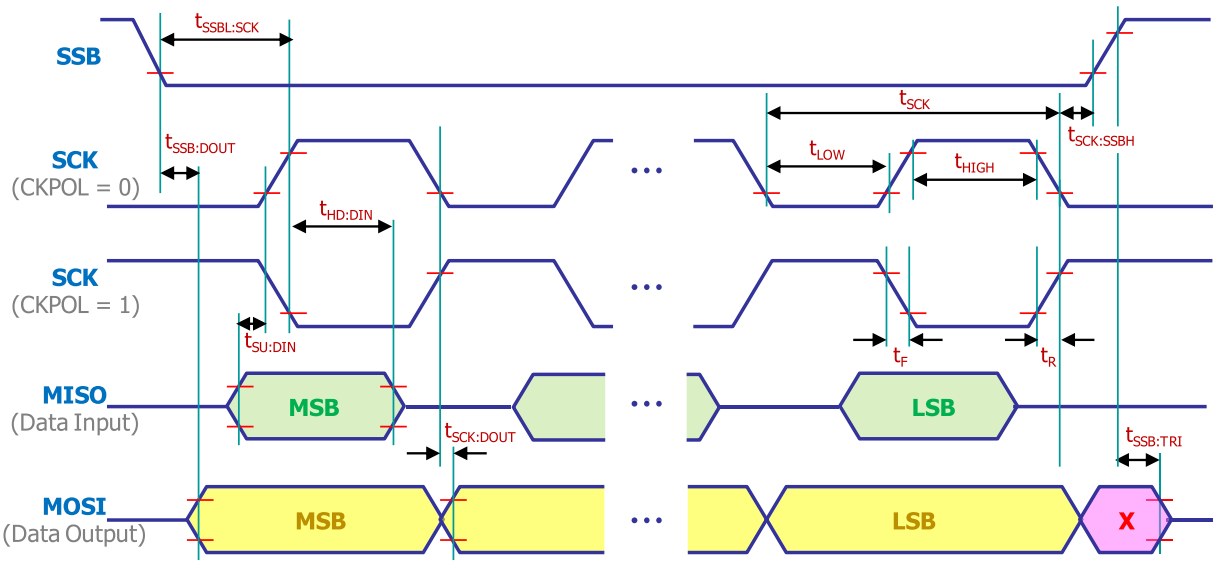


Symbol	Characteristics		Min. [ns]	Max. [ns]	Conditions
t_{HIGH}	Clock High Time	100kHz Mode	4,000	-	Minimum Frequency : 1MHz
		400kHz Mode	600	-	Minimum Frequency : 5MHz
t_{LOW}	Clock Low Time	100kHz Mode	4,700	-	Minimum Frequency : 1MHz
		400kHz Mode	1,300	-	Minimum Frequency : 5MHz
$t_{SU:DAT}$	Data Input Setup Time	100kHz Mode	250	-	
		400kHz Mode	100	-	
$t_{HD:DAT}$	Data Input Hold Time	100kHz Mode	0	-	
		400kHz Mode	0	900	
t_{AA}	Data Valid from Clock	100kHz Mode	-	3,500	
		400kHz Mode	-	-	
t_{BF}	BUS Free Time	100kHz Mode	4,700	-	
		400kHz Mode	1,300	-	
t_R	SDA & SCL Rising Time	100kHz Mode	-	1,000	The Range of Cb is from 10pF to 400pF
		400kHz Mode	2.0 + 0.1Cb	300	
t_F	SDA & SCL Falling Time	100kHz Mode	-	300	The Range of Cb is from 10pF to 400pF
		400kHz Mode	2.0 + 0.1Cb	300	

9 SPI Timing Characteristics

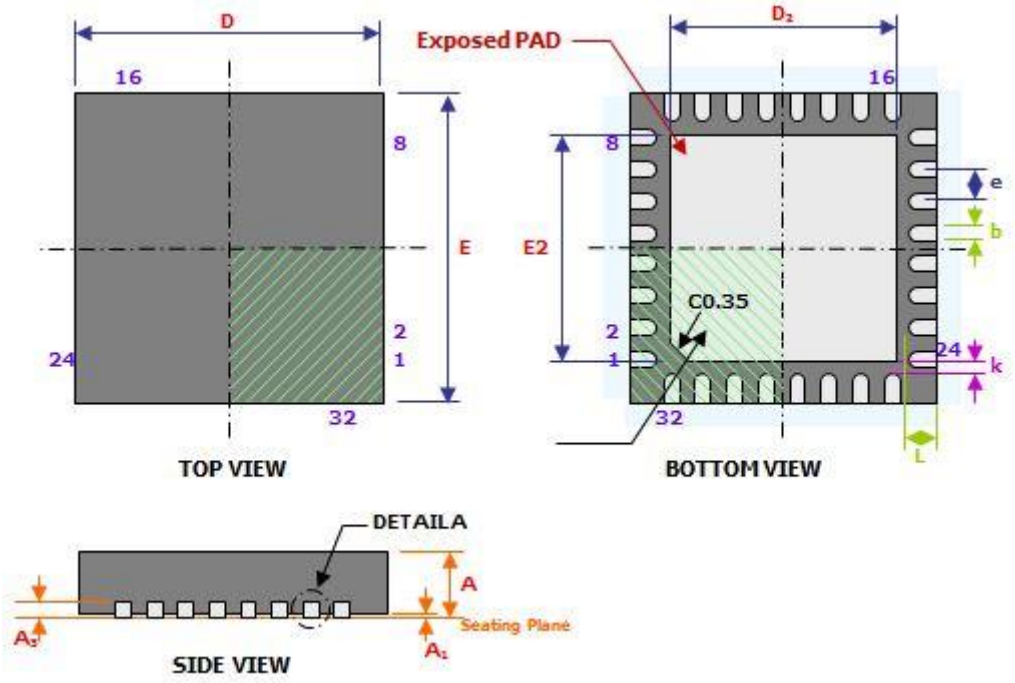


Symbol	Description	Mode	Min. [ns]	Typ. [ns]	Max. [ns]
t_{SCK}	SCK Period Time (using SFR 'SPICK')	Master	-	$F_{OSC}/2$ ~ $F_{OSC}/256$	-
t_{HIGH}, t_{LOW}	SCK High / Low	Master	-	50% Duty Cycle	-
t_F, t_R	SCK Rise / Fall Time	Master	-	3.6	-
$t_{SU:DIN}$	Data Input Setup Time	Master	-	10	-
$t_{HD:DIN}$	Data Input Hold Time	Master	-	10	-
$t_{DOUT:SCK}$	Data Output to SCK	Master	-	0.5 X t_{SCK}	-
$t_{SCK:DOUT}$	SCK to Data Output	Master	-	10	-
$t_{SCK:DOUTH}$	SCK to Data Output High	Master	-	10	-



Symbol	Description	Mode	Min. [ns]	Typ. [ns]	Max. [ns]
$t_{SSB:DOUT}$	SSB Low to Data Output	Slave	-	15	-
T_{SCK}	SCK Period Time	Slave	4 X t_{Sys}	-	-
t_{HIGH}, t_{LOW}	SCK High / Low	Slave	2 X t_{Sys}	-	-
t_F, t_R	SCK Rise / Fall Time	Slave	-	1,600	-
$t_{SU:DIN}$	Data Input Setup Time	Slave	10	-	-
$t_{HD:DIN}$	Data Input Hold Time	Slave	t_{Sys}	-	-
$t_{SCK:DOUT}$	SCK to Data Output	Slave	-	15	-
$t_{SCK:SSBH}$	SCK to SSB High	Slave	20	-	-
$t_{SSB:TRI}$	SSB High to Tri-state	Slave	-	10	-
$t_{SSBL:SCK}$	SSB Low to SCK	Slave	20	-	-

10 32-pin QFN Package Dimension



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A_1	0.00	0.02	0.05
A_3		0.20 REF	
D		5.00 BSC	
E		5.00 BSC	
D_2	3.60	3.70	3.80
E_2	3.60	3.70	3.80
b	0.18	0.25	0.30
e		0.50 BSC	
L	0.30	0.40	0.50

Notes:

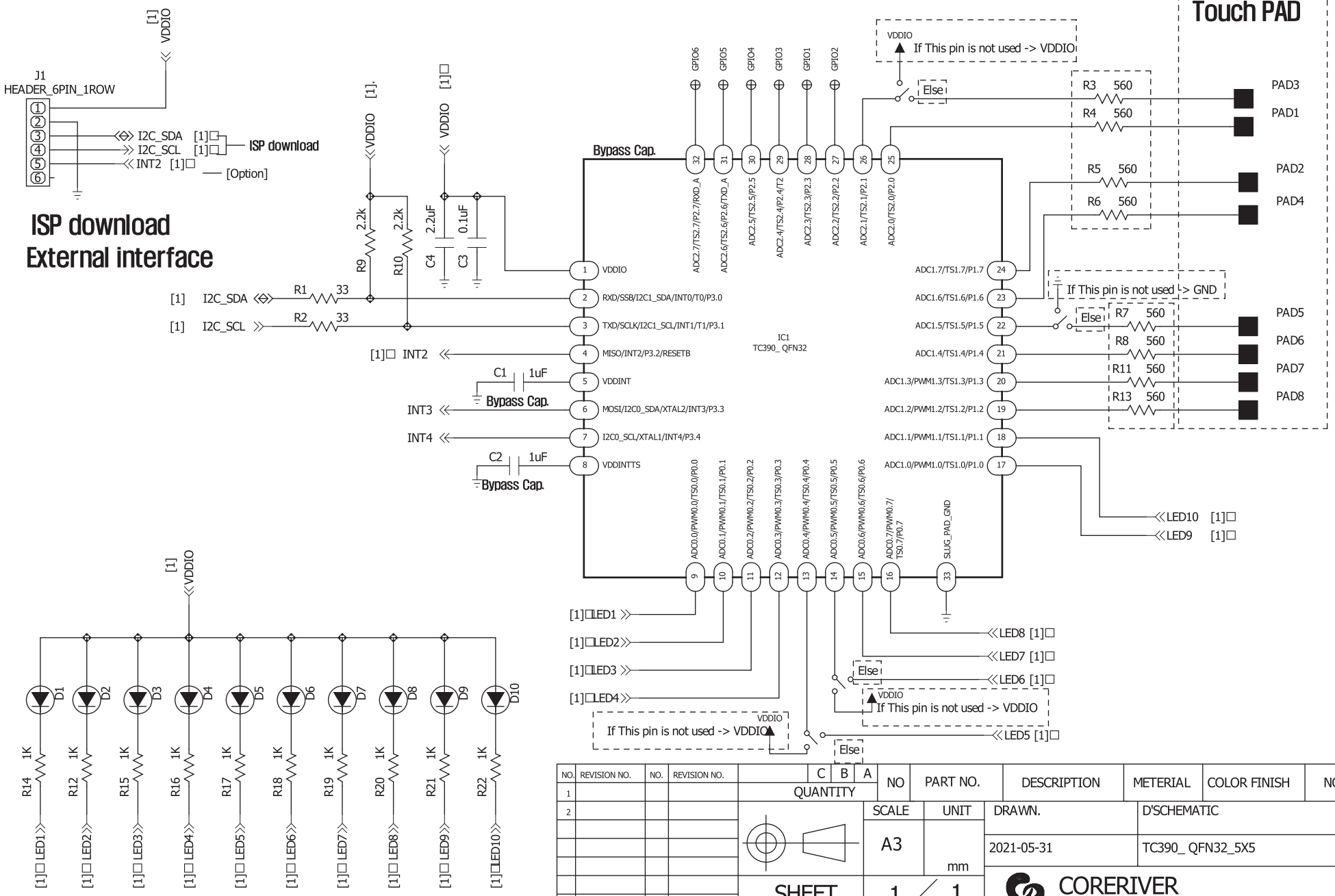
1. All Dimension are in mm. Angles in Degrees.

2. Dimension b applies to Plated Terminal & is measured.

3. BSC : Basic Dimension. Theoretically exact value shown without tolerances.
REF : Reference Dimension, Usually without tolerance, for information purpose only.

TouchCore390_QFN32_5X5

>> VDDIO (Operating Voltage) : +2.7V to +3.6V



NO.	REVISION NO.	NO.	REVISION NO.		C	B	A	NO	PART NO.	DESCRIPTION	METERIAL	COLOR FINISH	NOTE
1				QUANTITY									
2													

SCALE	UNIT	DRAWN.	D'SCHEMATIC
A3	mm	2021-05-31	TC390_ QFN32_5X5
SHEET	1 / 1	CORERIVER	